IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LINEAR TECHNOLOGY CORPORATION	)	
Plaintiff,	)	C. A. No. ______
v.	)	**DEMAND FOR JURY TRIAL**
MONOLITHIC POWER SYSTEMS, INC.	)	**PUBLIC VERSION**
Defendant.	)	

COMPLAINT

Plaintiff, Linear Technologies Corporation ("Linear"), by its attorneys, brings this action against the defendant Monolithic Power Systems, Inc. ("Monolithic") for breach of contract and patent infringement and alleges as follows:

JURISDICTION AND VENUE

1. This action for patent infringement arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction under 28 U.S.C. § 1338. This Court has supplemental jurisdiction over Linear's breach of contract claims under 28 U.S.C. § 1367.

2. Venue is proper under 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b) because both parties reside in this district and defendant's acts of infringement and breach of contract have occurred in this district. Additionally, under the express terms of the contract that Monolithic breached, the parties agreed that any dispute arising thereunder would be brought in Delaware.

PARTIES AND PATENTS AT ISSUE

3. Linear is a Delaware corporation with its U.S. headquarters at 1630 McCarthy Boulevard, Milpitas, California 95035.

4. Upon information and belief, Monolithic was first incorporated in 1997 in California, was reincorporated in Delaware in 2004, and has its headquarters in Los Gatos, California.

5. On January 2, 1996, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 5,481,178 ("the '178 patent"), entitled "Control Circuit and Method for Maintaining High Efficiency Over Broad Current Ranges in a Switching Regulator Circuit," in the names of Milton E. Wilcox and Randy Flatness, who assigned their entire rights and interests in the '178 patent to Linear. A true and correct copy of the '178 patent is attached as Exhibit A.

6. On June 17, 2003, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,580,258 B2 ("the '258 patent"), entitled "Control Circuit and Method for Maintaining High Efficiency Over Broad Current Ranges in a Switching Regulator Circuit," in the names of Milton E. Wilcox and Randy Flatness, who assigned their entire rights and interests in the '258 patent to Linear. A true and correct copy of the '258 patent is attached as Exhibit B.

7. Monolithic has had actual notice and constructive notice pursuant to 35 U.S.C. §287 of the '178 and '258 patents.

COUNT I
BREACH OF THE SETTLEMENT AGREEMENT

8. On or about August 17, 2004, the United States International Trade Commission instituted an investigation of Monolithic under Section 337 of the Tarriff Act of 1930, as amended (19 U.S.C. § 1337) for unfair methods of competition in connection with Monolithic's importation into the United States of products that infringed the '178 patent and the '258 patent. (The "ITC Investigation").

9. On or about September 29, 2005, Linear and Monolithic entered into a Settlement Agreement and License Agreement ("the Settlement Agreement"), and a Consent Order Stipulation, pursuant to which the parties settled the issues between them in the ITC investigation. A true and correct copy of the Settlement Agreement and the Consent Order Stipulation is attached as Exhibit C. On September 30, 2005, the parties filed a "Joint Motion to Terminate Investigation Based Upon A Settlement Agreement and Consent Order" to terminate the ITC Investigation.

10. In the Settlement Agreement, Linear granted Monolithic **REDACTED**:

REDACTED

11. Under the terms of the Settlement Agreement, **REDACTED**

12. Additionally, Monolithic **REDACTED**

13. The Settlement Agreement additionally states **REDACTED**:

REDACTED

14. Monolithic further agreed that **REDACTED**

15. Upon information and belief, after the effective date of the Settlement Agreement, Monolithic has been and continues to sell products that infringe the '178 and '258 patents.

16. Monolithic's sales of such infringing products, including the MP1543 Synchronous Rectified Step-Up Converter, constitutes a breach of the Settlement Agreement. Such sales have caused Linear to sustain monetary and other damages.

COUNT II
PATENT INFRINGEMENT

17. Linear restates and realleges paragraphs 1-16 above as if fully set forth herein.

18. Upon information and belief, Monolithic has been and is infringing, inducing infringement and/or contributing to the infringement of one or more claims of the '178 and '258 patents by making, using, selling and/or offering to sell in, and importing into, the United States voltage regulator circuits, including, the MP1543 Synchronous Rectified Step-Up Converter, which embody, incorporate or otherwise practice the claimed invention of the '178 and '258 patents.

19. As a direct and proximate result of Monolithic's infringement of the '178 and '258 patents, Linear has been and continues to sustain monetary and other damages, including the loss of revenues in an amount to be determined at trial.

20. Linear has been and continues to be irreparably harmed by Monolithic's infringement of the '178 and '258 patents. Monolithic's infringing activities will continue unless enjoined by this Court.

21. Upon information and belief, Monolithic's infringement of the '178 and '258 patents has been willful and deliberate.

RELIEF REQUESTED

Linear, therefore, respectfully requests that this Court enter a judgment against defendant Monolithic:

A. Declaring that Monolithic has infringed the '178 patent;

B. Declaring that Monolithic's infringement of the '178 patent has been willful;

C. Declaring that Monolithic has infringed the '258 patent;

D. Declaring that Monolithic's infringement of the '258 patent has been willful;

E. Awarding preliminary and permanent injunctive relief precluding Monolithic, its subsidiaries, officers, agents, servants, employees, and all other persons in active concert or participation with each from further infringement of the '178 and '258 patents;

F. Awarding Linear its damages sustained as a result of Monolithic's infringement of Linear's '178 and '258 patents with interest;

G. Trebling the damages Linear incurred as a result of Monolithic's willful and deliberate infringement of Linear's '178 and '258 patents;

H. Declaring this action an exceptional case under 35 U.S.C. § 285, and awarding Linear its costs and attorney fees;

I. Declaring that Monolithic has breached the express terms of the Settlement Agreement;

J. Awarding Linear liquidated damages **REDACTED**

K. Granting an accounting for the damages to Linear arising out of Monolithic's infringing activities and breach of the Settlement Agreement together with interest and costs, and awarding such damages to Linear.

L. Granting such other relief as the Court deems just and proper.

JURY DEMAND

Under Rule 38(b) of the Federal Rules of Civil Procedure, Linear respectfully requests a jury trial on all issues triable to a jury in this matter.

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530621

EXHIBIT A

US005481178A

United States Patent [19]

Wilcox et al.

[11] Patent Number: 5,481,178

[45] Date of Patent: Jan. 2, 1996

[54] **CONTROL CIRCUIT AND METHOD FOR MAINTAINING HIGH EFFICIENCY OVER BROAD CURRENT RANGES IN A SWITCHING REGULATOR CIRCUIT**

[75] Inventors: **Milton E. Wilcox**, Saratoga; **Randy G. Flatness**, Los Gatos, both of Calif.

[73] Assignee: **Linear Technology Corporation**, Milpitas, Calif.

[21] Appl. No.: **36,047**

[22] Filed: **Mar. 23, 1993**

[51] **Int. Cl.**[6] **G05F 1/618**

[52] **U.S. Cl.** **323/287**; 323/224

[58] **Field of Search** 323/259, 344, 323/271, 268, 275, 285, 350, 274, 277, 287, 284, 224

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,395,675	7/1983	Toumani	323/271
4,578,630	3/1986	Grosch	323/271
4,706,177	11/1987	Josephson	363/24
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5,184,729	2/1993	Fung et al.	341/144

FOREIGN PATENT DOCUMENTS

0428377 5/1991 European Pat. Off. .

OTHER PUBLICATIONS

"LT1432 5 V High Efficiency Step–Down Switching Regulator Controller," Data Sheet published by Linear Technology Corporation in the *1992 Linear Databook Supplement*, Milpitas, Calif. , pp. 4–145 to 4–171.

"Max 782/Max 786 Notebook Computer Power Supplies," Advance Information Data Sheet published by Maxim Integrated Products, Feb. 1993, Sunnyvale, Calif., pp. 1–8.

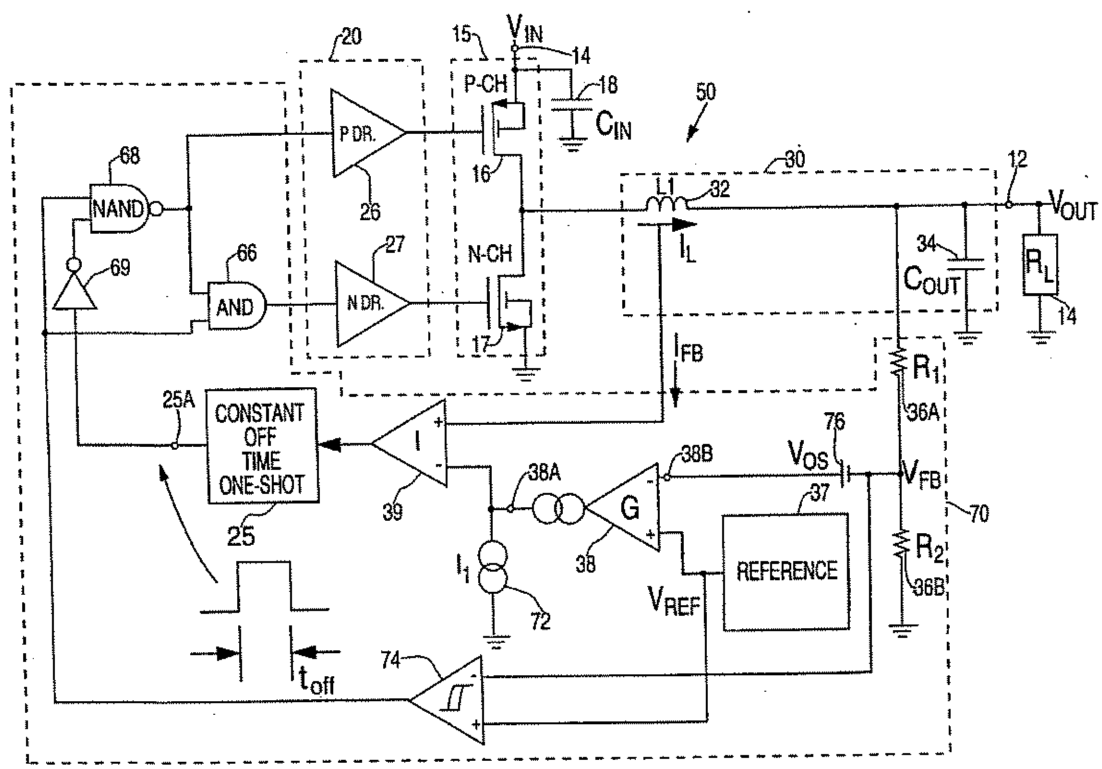
"ML4873 Battery Power Control IC," Advance Information Data Sheet published by Micro Linear Corporation, dated Mar. 15, 1993, San Jose, Calif., pp. 1–8.

Primary Examiner—Peter S. Wong
Assistant Examiner—Shawn Riley
Attorney, Agent, or Firm—Fish & Neave; Mark D. Rowland; Robert W. Morris

[57] **ABSTRACT**

A circuit and method for controlling a switching voltage regulator having (1) a switch including one or more switching transistors and (2) an output adapted to supply current at a regulated voltage to a load including an output capacitor. The circuit and method generates a control signal to turn said one or more switching transistors OFF under operating conditions when the voltage at the output is capable of being maintained substantially at the regulated voltage by the charge on the output capacitor. Such a circuit and method increases the efficiency of the regulator circuit particularly at low average current levels.

57 Claims, 10 Drawing Sheets



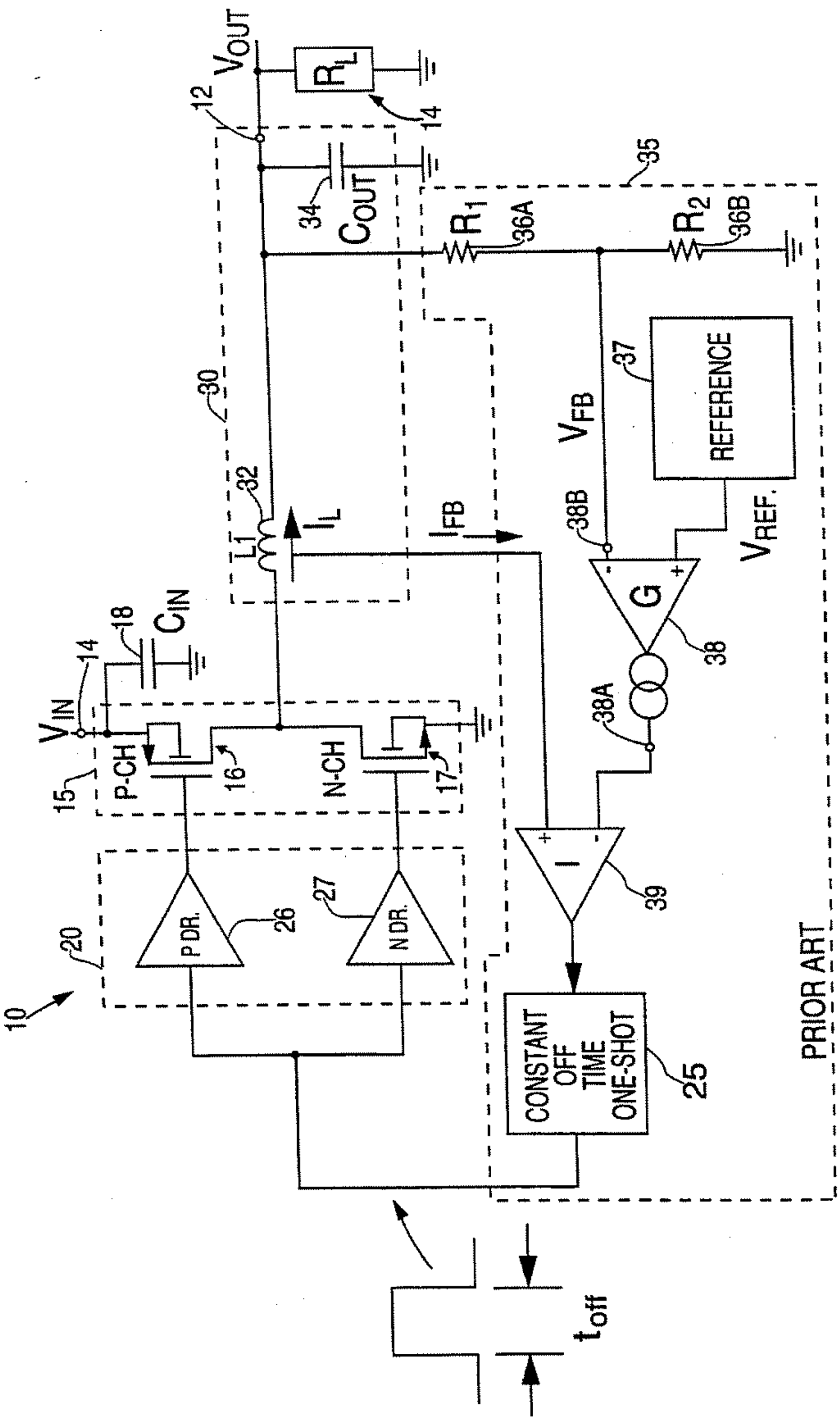
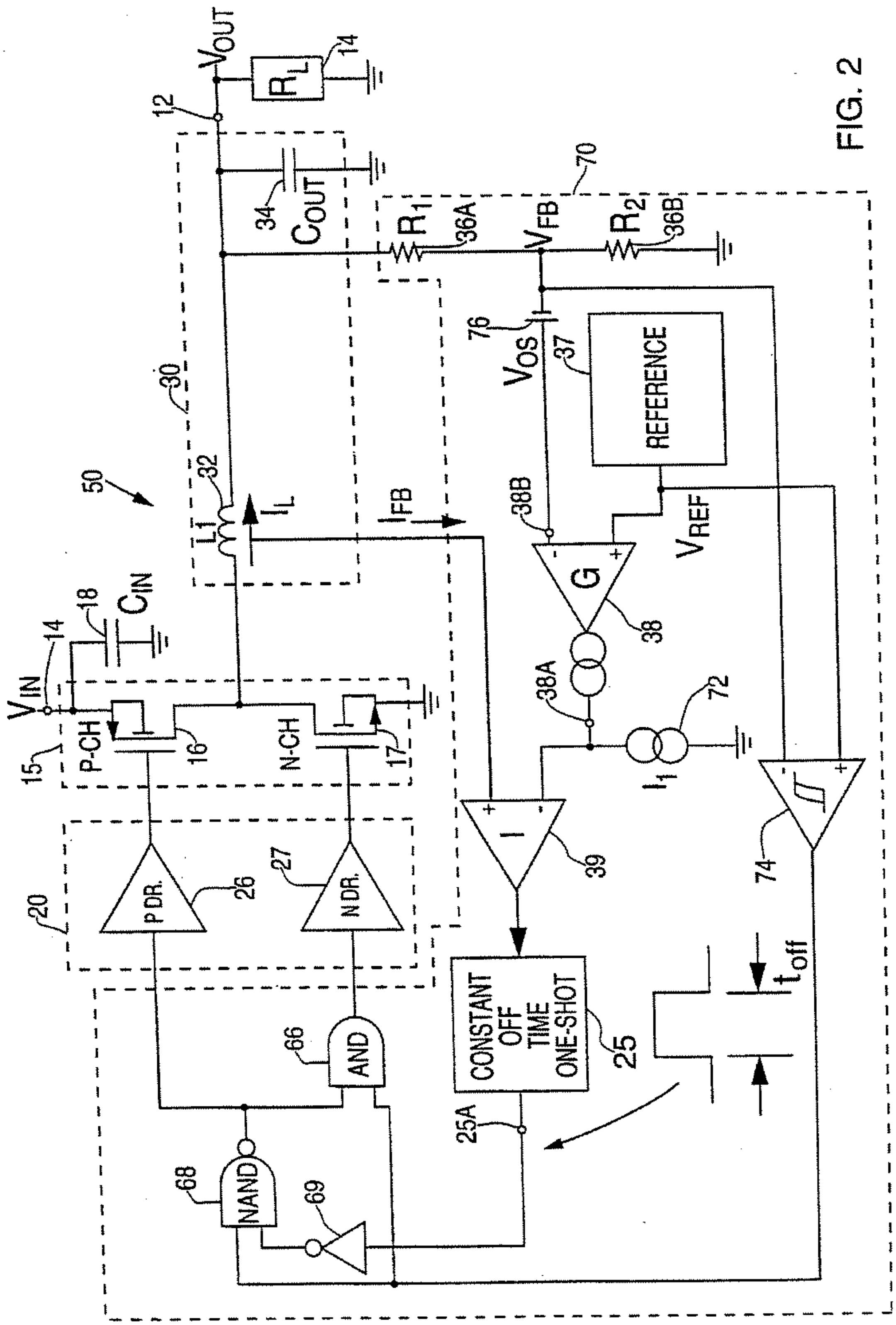

V_{OUT}
R_L
12
14
34
C_{OUT}
35
R_1
36A
R_2
36B
30
37
REFERENCE
V_{FB}
32
L1
I_L
I_{FB}
38B
$V_{REF.}$
G
38
18
C_{IN}
14
V_{IN}
38A
15
P-CH
16
N-CH
17
I
39
20
P DR.
26
27
N DR.
10
CONSTANT OFF TIME ONE-SHOT
25
PRIOR ART
t_{off}

FIG. 1



V_{OUT}
R_L
C_{OUT}
R_1
V_{FB}
R_2
V_{OS}
REFERENCE
V_{REF}
$L1$
I_L
I_{FB}
V_{IN}
C_{IN}
P-CH
N-CH
P DR.
N DR.
G
I
I_1
AND
NAND
CONSTANT OFF TIME ONE-SHOT
t_{off}

FIG. 2

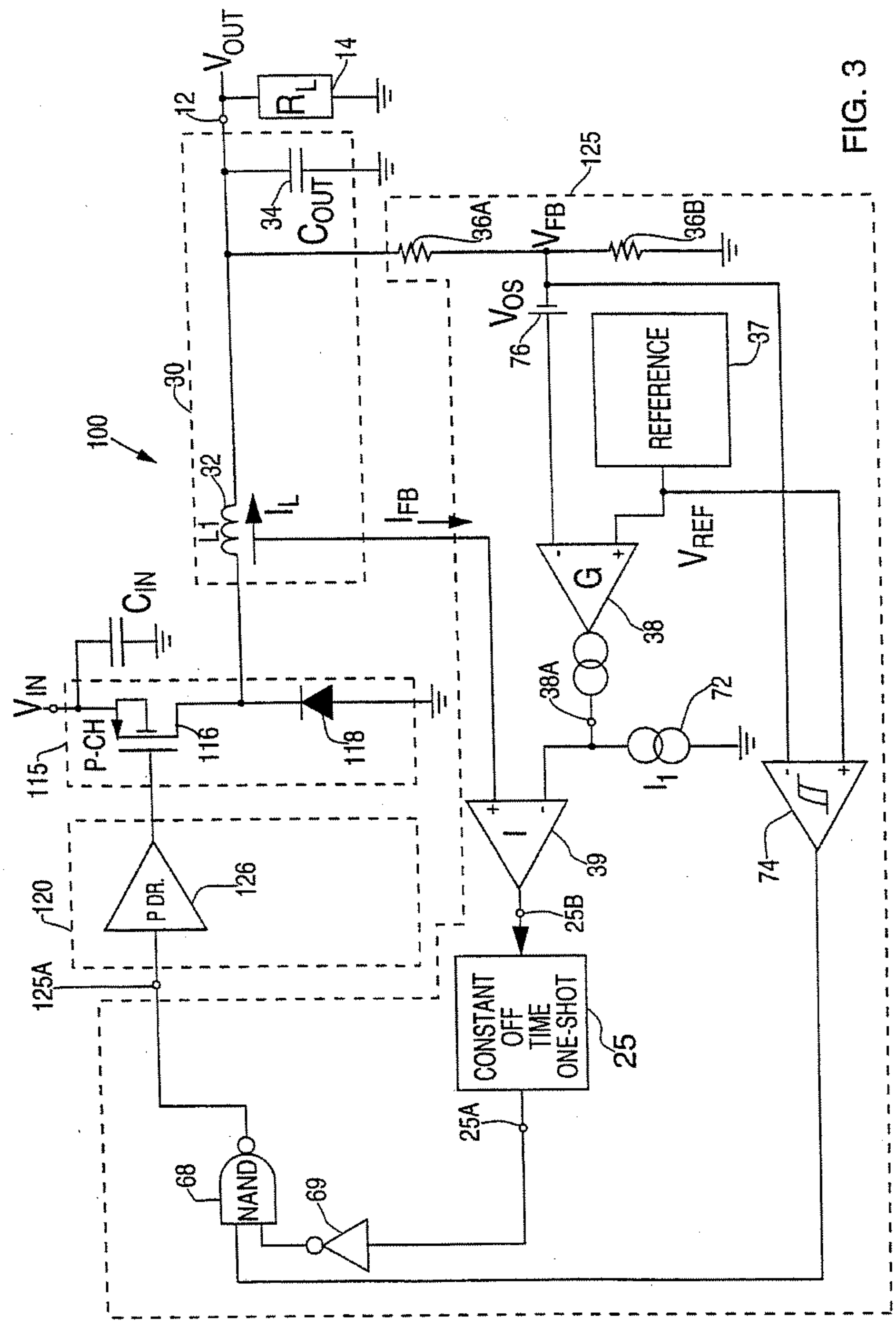
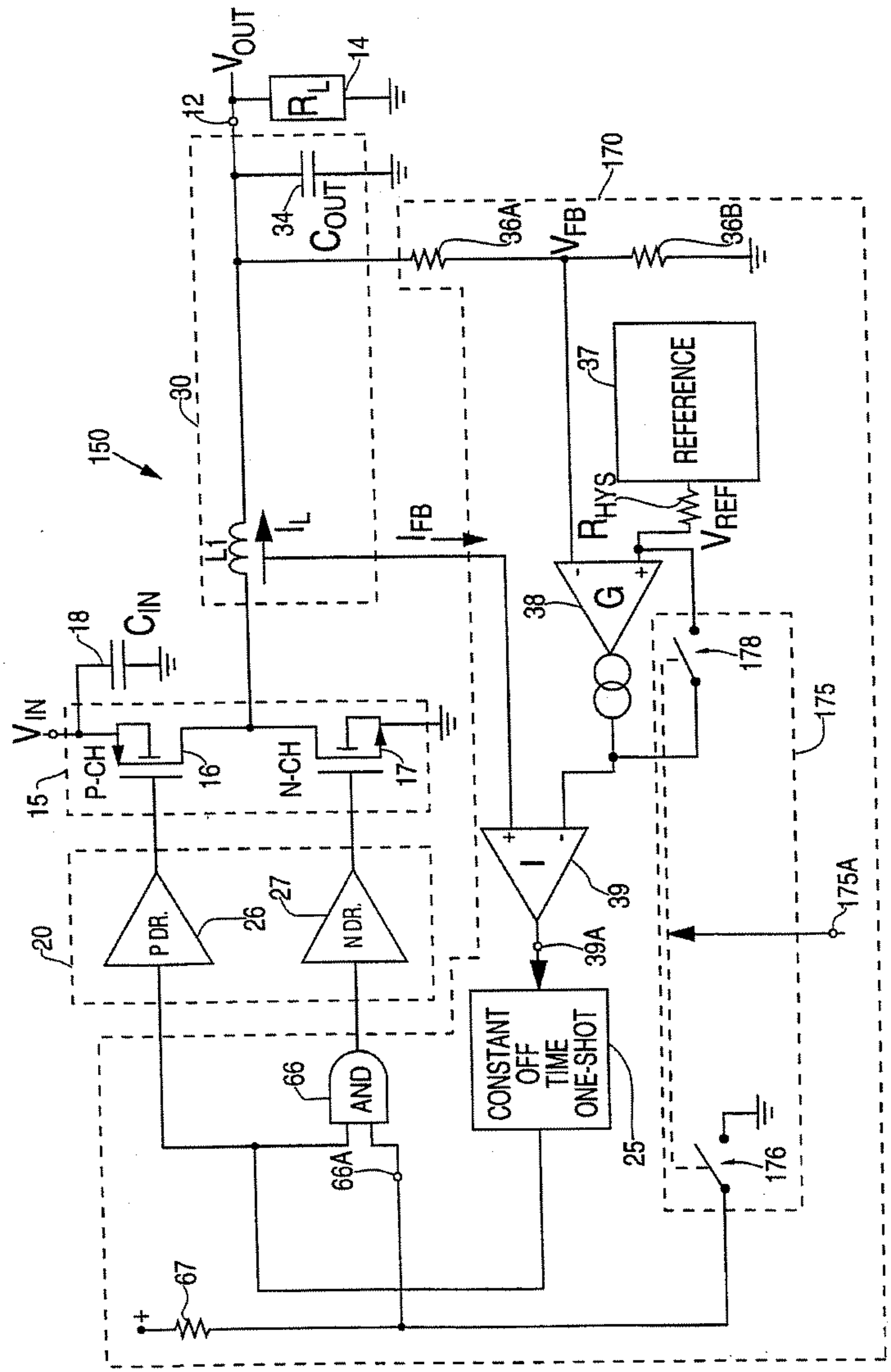
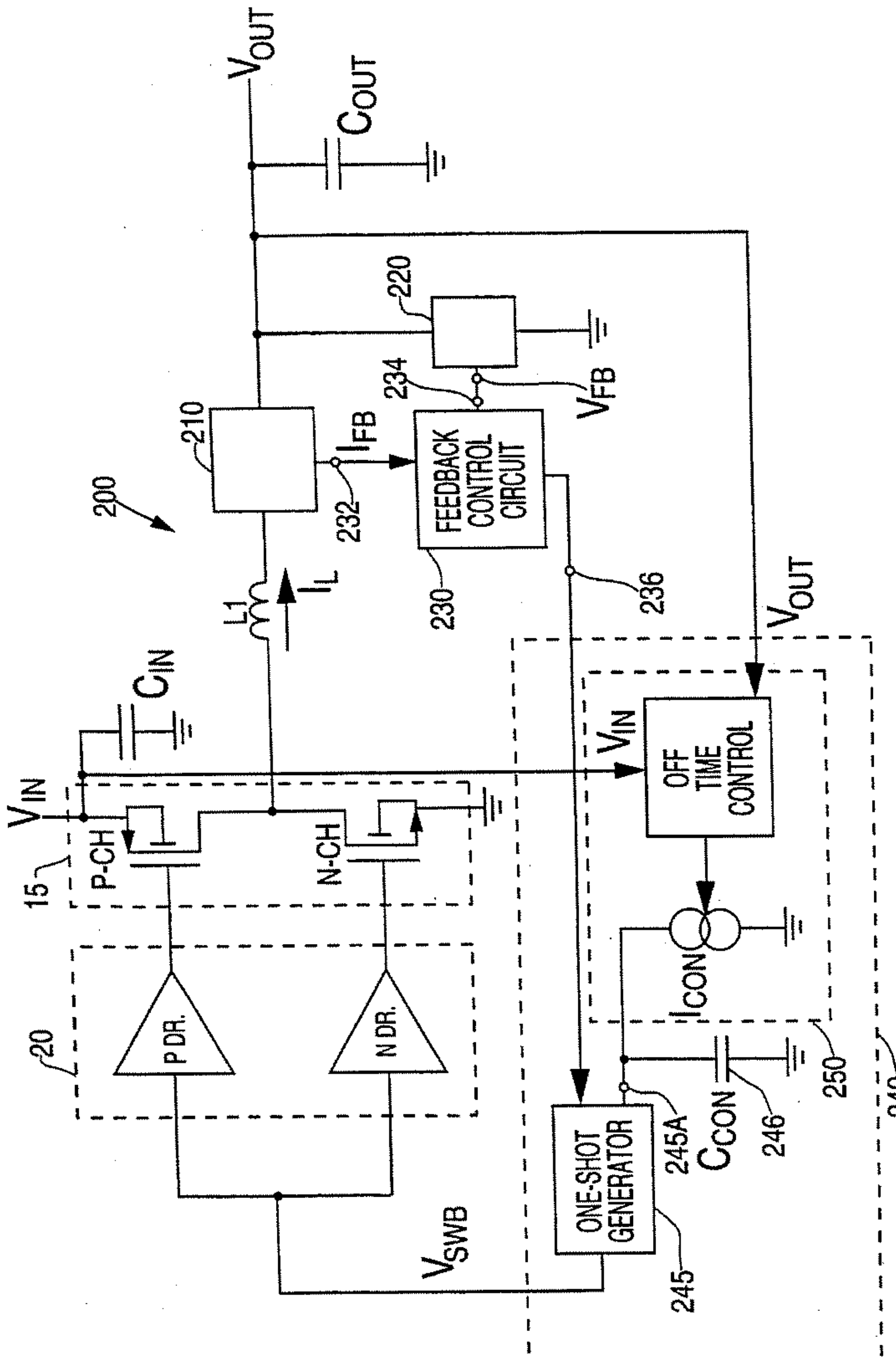

V_{OUT}
12
14
R_L
125
34
C_{OUT}
36A
V_{FB}
36B
V_{OS}
76
REFERENCE
37
30
100
32
L1
I_L
I_{FB}
V_{REF}
G
38
C_{IN}
V_{IN}
38A
72
I_1
P-CH
115
116
118
39
74
120
P DR.
126
25B
CONSTANT OFF TIME ONE-SHOT
25
125A
25A
68
NAND
69

FIG. 3



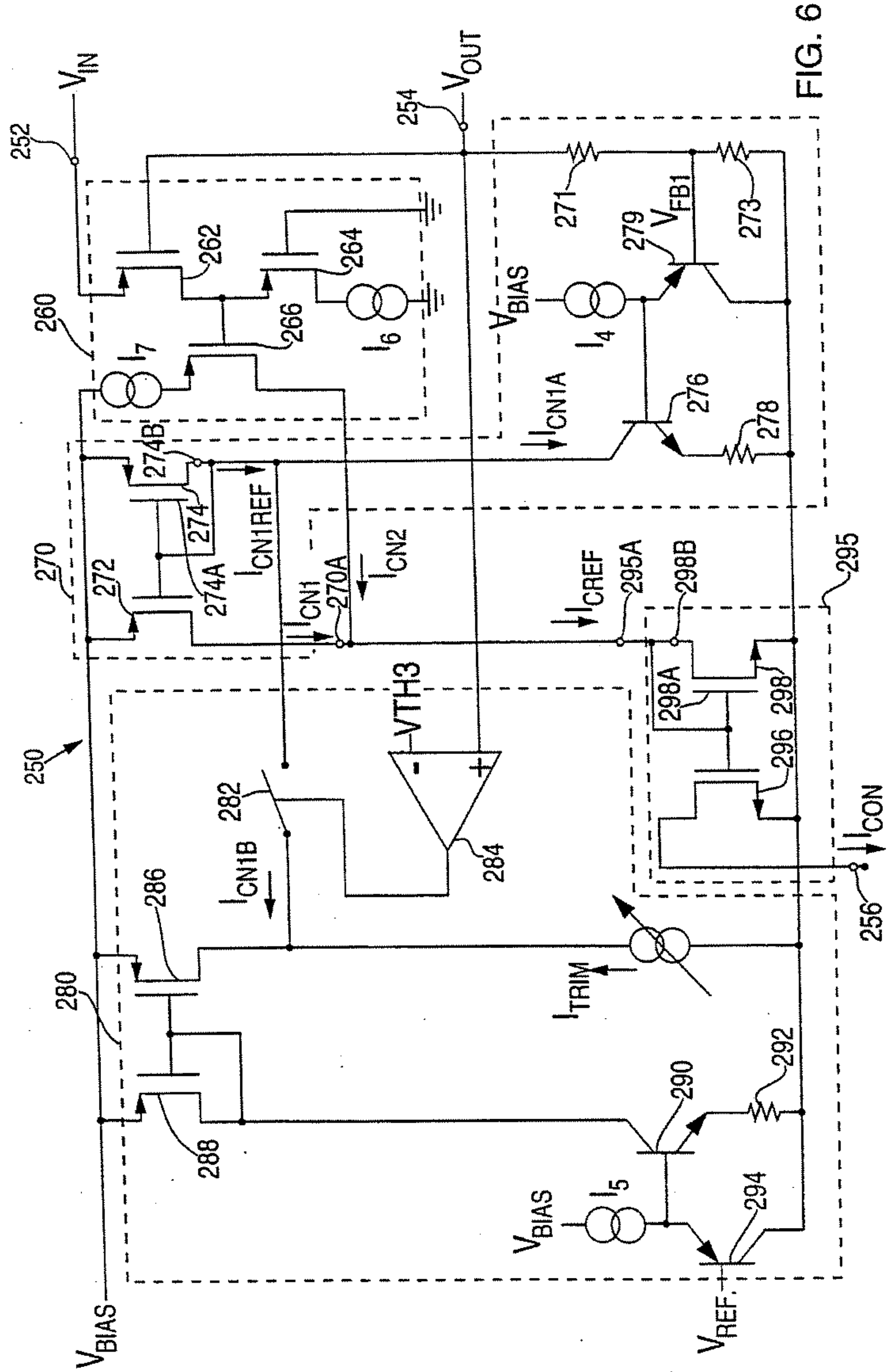
V_{OUT}
14
R_L
12
170
34
C_{OUT}
36A
V_{FB}
36B
37
REFERENCE
30
150
R_{HYS}
V_{REF}
I_L
L1
I_{FB}
38
G
18
C_{IN}
V_{IN}
178
175
15
P-CH
16
N-CH
17
39
I
175A
20
P DR.
26
27
N DR.
39A
66
AND
CONSTANT OFF TIME ONE-SHOT
25
66A
176
67

FIG. 4



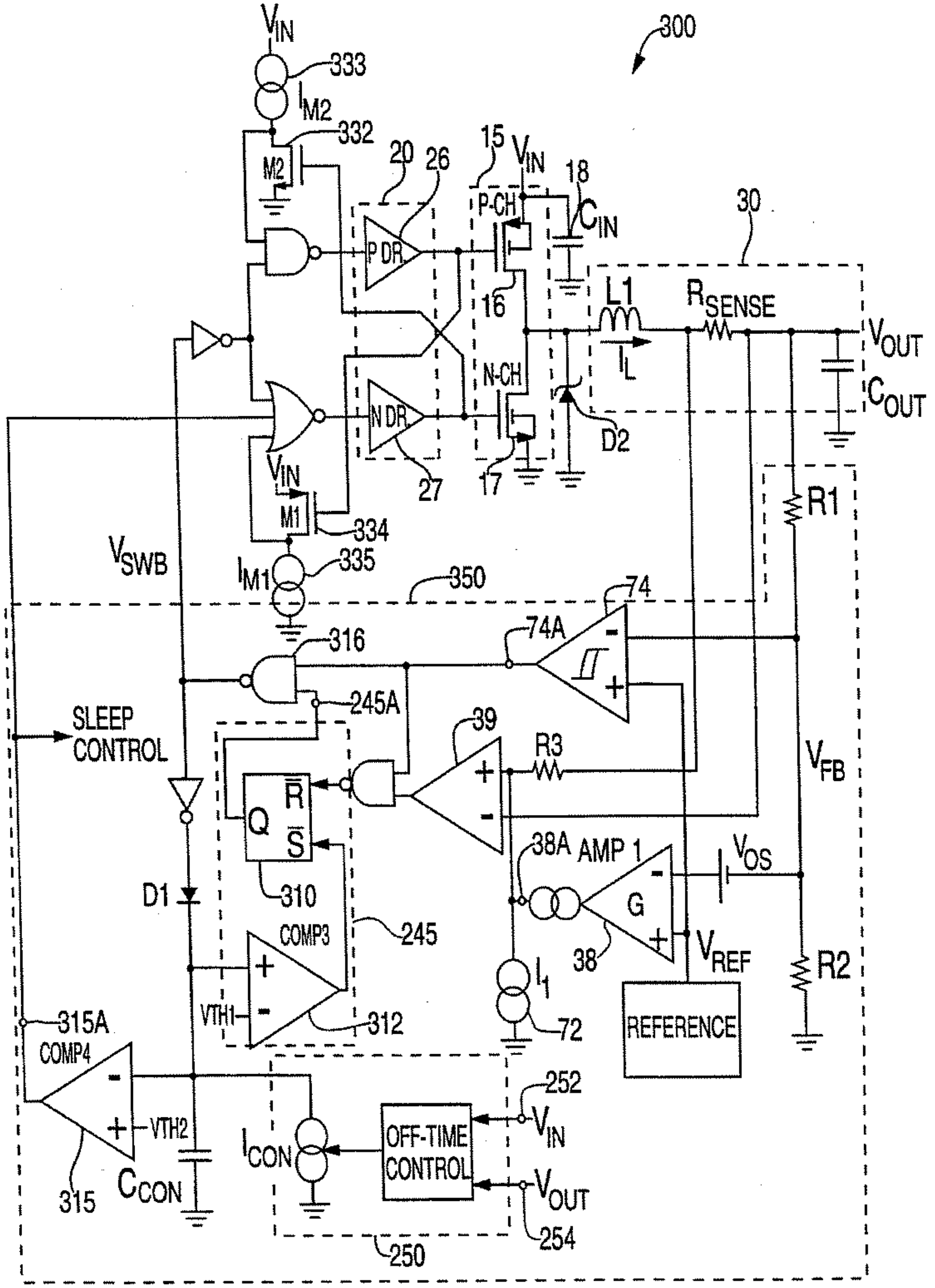
V_{OUT}
C_{OUT}
220
234
V_{FB}
210
I_{FB}
200
232
FEEDBACK CONTROL CIRCUIT
230
236
V_{OUT}
L1
I_L
C_{IN}
V_{IN}
OFF TIME CONTROL
V_{IN}
P-CH
N-CH
15
I_{CON}
20
P DR.
N DR.
250
240
245A
C_{CON}
246
ONE-SHOT GENERATOR
245
V_{SWB}

FIG. 5



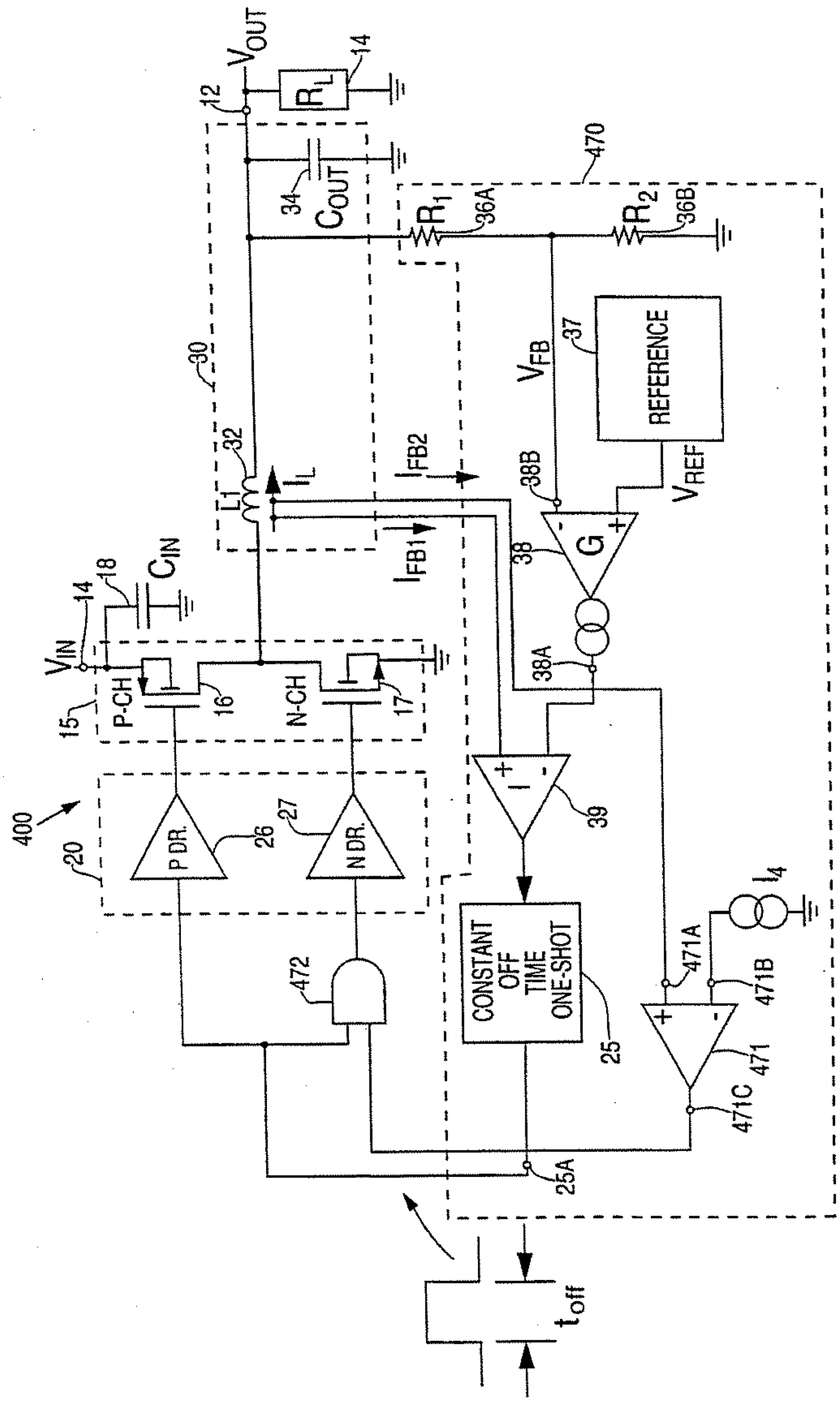
VIN
252
VOUT
254
260
262
264
266
I7
I6
VBIAS
I4
271
273
279
VFB1
276
278
ICN1A
270
272
274
274A
274B
ICN1REF
ICN1
270A
ICN2
ICREF
295A
298B
295
298A
298
296
ICON
256
VTH3
282
284
ICN1B
286
280
288
ITRIM
290
292
I5
VBIAS
294
VREF
VBIAS
250

FIG. 6



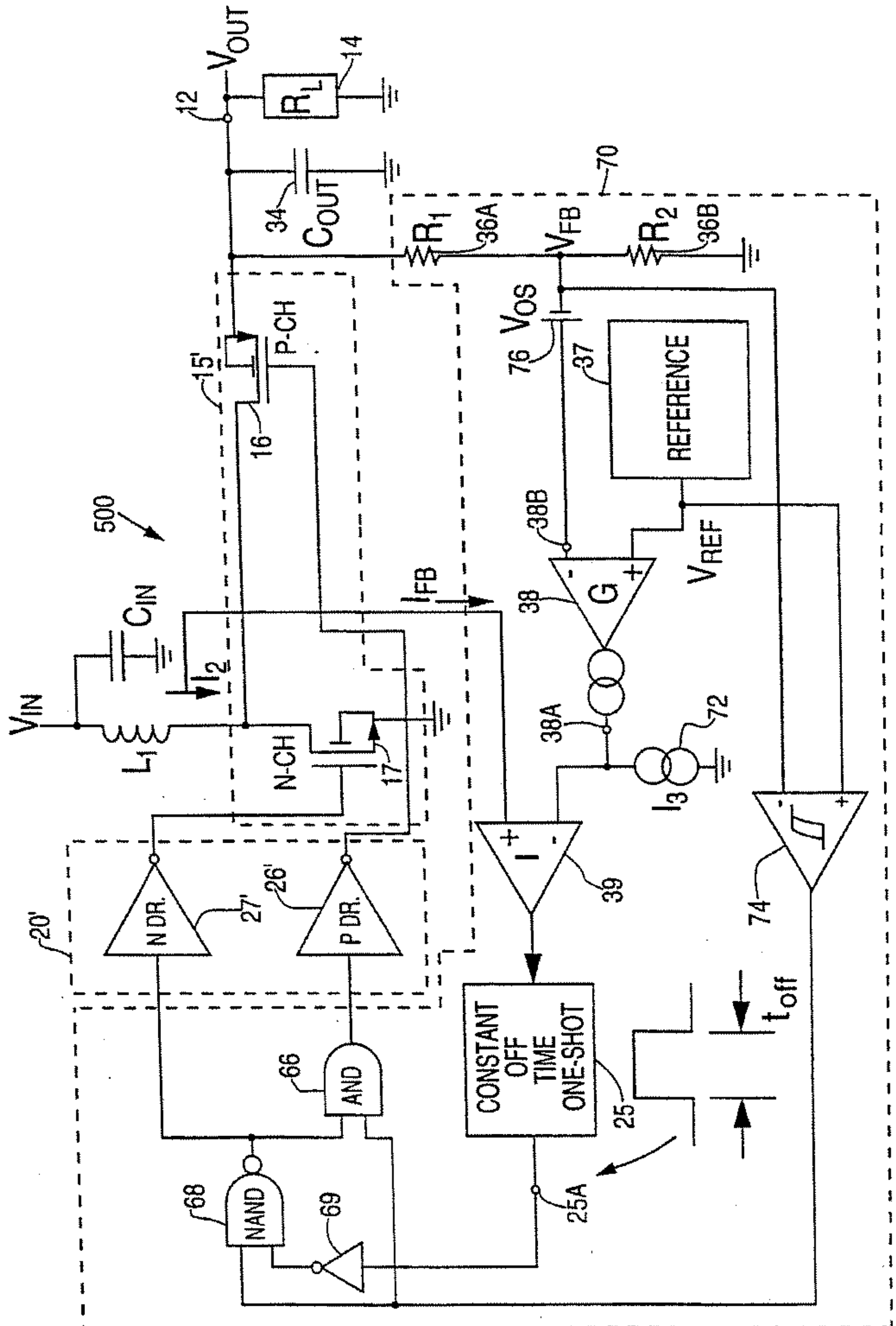
300
VIN
333
IM2
332
M2
20
26
15
VIN
18
CIN
P-CH
P DR
30
16
L1
RSENSE
VOUT
IL
N-CH
N DR
COUT
D2
VIN
27
17
M1
334
R1
VSWB
IM1
335
350
74
74A
316
245A
SLEEP
CONTROL
39
R3
VFB
Q
R
S
38A
AMP 1
VOS
G
D1
310
COMP3
245
38
VREF
R2
I1
VTH1
312
72
REFERENCE
315A
COMP4
252
VIN
VTH2
ICON
OFF-TIME
CONTROL
315
CCON
VOUT
254
250

FIG. 7



V_{OUT}
R_L
14
12
C_{OUT}
34
470
R_1
36A
R_2
36B
REFERENCE
37
V_{FB}
30
32
L1
I_L
I_{FB2}
I_{FB1}
38B
V_{REF}
G
38
C_{IN}
18
14
V_{IN}
P-CH
16
N-CH
17
15
38A
I
39
400
20
P DR.
26
27
N DR.
CONSTANT OFF TIME ONE-SHOT
25
I_4
471A
471B
471
471C
472
25A
t_{off}

FIG. 8



VOUT
12
14
RL
34
COUT
70
R1
36A
VFB
R2
36B
VOS
76
37
REFERENCE
15'
P-CH
16
500
38B
VREF
G
38
IFB
CIN
VIN
I2
L1
N-CH
17
38A
72
I3
I
39
74
20'
N DR.
27'
26'
P DR.
CONSTANT OFF TIME ONE-SHOT
toff
25
66
AND
68
NAND
69
25A

FIG. 9

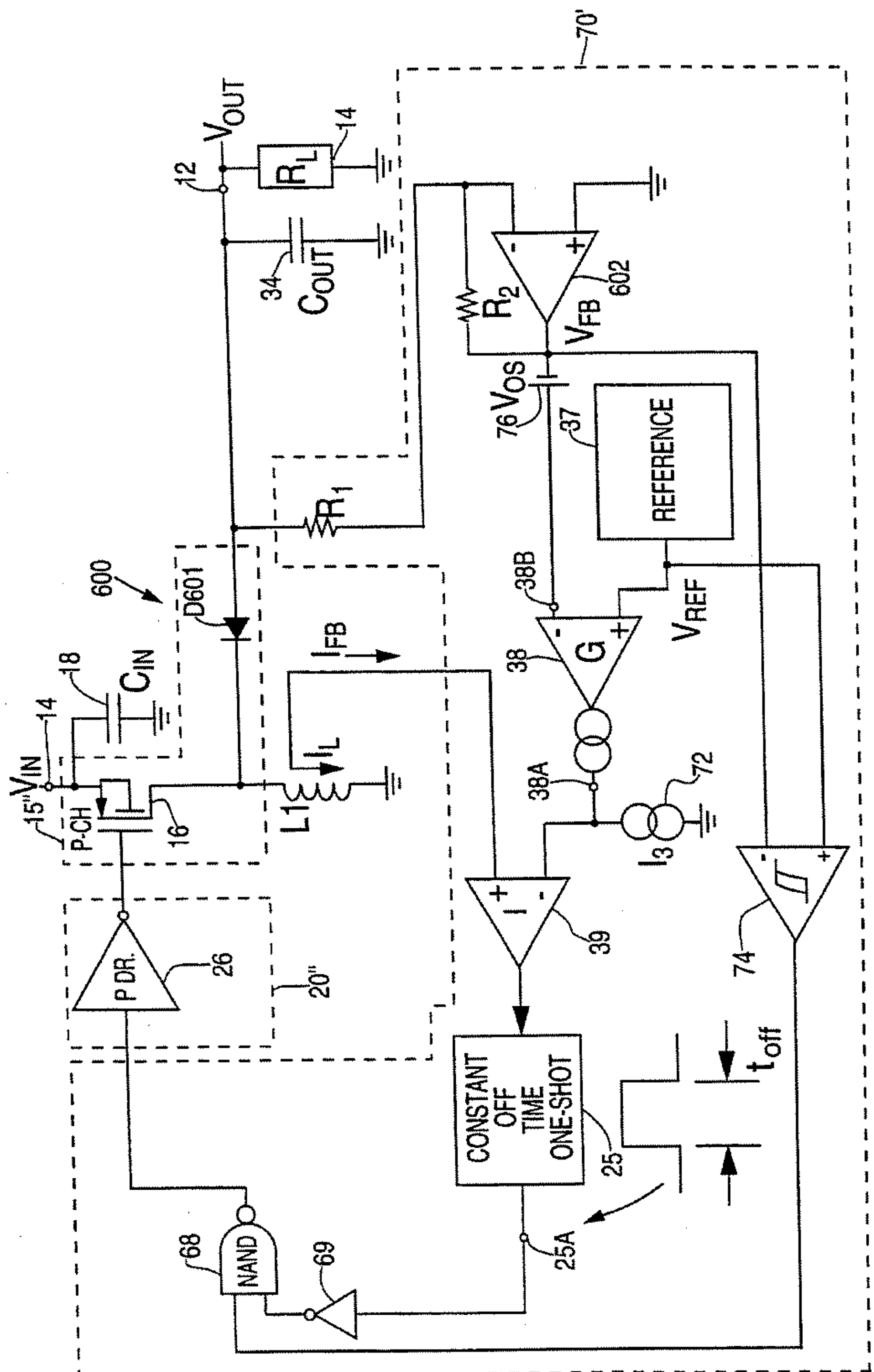

70'
V_{OUT}
12
R_L
14
34
C_{OUT}
R_2
602
V_{FB}
76
V_{OS}
37
REFERENCE
R_1
600
D601
38B
38
G
V_{REF}
18
C_{IN}
14
V_{IN}
15"
P-CH
16
I_{FB}
I_L
L1
38A
72
I_3
39
I
74
P DR.
26
20"
CONSTANT OFF TIME ONE-SHOT
25
t_{off}
25A
68
NAND
69

FIG. 10

CONTROL CIRCUIT AND METHOD FOR MAINTAINING HIGH EFFICIENCY OVER BROAD CURRENT RANGES IN A SWITCHING REGULATOR CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a switching regulator circuit. More particularly, the present invention relates to a control circuit and method for maintaining high efficiency over broad current ranges in a switching regulator circuit.

The purpose of a voltage regulator is to provide a predetermined and constant output voltage to a load from a poorly-specified and fluctuating input voltage source. Generally, there are two different types of regulators: series regulators and switching regulators.

The series regulator employs a pass element (e.g., a power transistor) coupled in series with a load and controls the voltage drop across the pass element in order to regulate the voltage which appears at the load. In contrast, the switching regulator employs a switch (e.g., a power transistor) coupled either in series or parallel with the load. The regulator controls the turning ON and turning OFF of the switch in order to regulate the flow of power to the load. The switching regulator employs inductive energy storage elements to convert the switched current pulses into a steady load current. Thus, power in a switching regulator is transmitted across the switch in discrete current pulses, whereas in a series regulator, power is transmitted across the pass element as a steady current flow.

In order to generate a stream of current pulses, switching regulators typically include control circuitry to turn the switch on and off. The switch duty cycle, which controls the flow of power to the load, can be varied by a variety of methods. For example, the duty cycle can be varied by either (1) fixing the pulse stream frequency and varying the ON or OFF time of each pulse, or (2) fixing the ON or OFF time of each pulse and varying the pulse stream frequency.

Which ever method is used to control the duty cycle, switching regulators are generally more efficient than series regulators. In series regulators, the pass element is generally operated in its linear region where the pass element conducts current continuously. This results in the continuous dissipation of power in the pass transistor. In contrast, in switching regulators, the switch is either OFF, where no power is dissipated by the switch, or ON in a low impedance state, where a small amount of power is dissipated by the switch. This difference in operation generally results in reduced amounts of average power dissipation in switching regulators.

The above difference in efficiency can be more apparent when there is a high input-output voltage difference across the regulator. For example, it would not be unusual for a series regulator to have an efficiency of less than 25 percent when a switching regulator could perform an equivalent function with an efficiency of greater than 75 percent.

Because of their improved efficiency over series regulators, switching regulators are typically employed in battery-operated systems such as portable and laptop computers and hand-held instruments. In such systems, when the switching regulator is supplying close to the rated output current (e.g., when a disk or hard drive is ON in a portable or laptop computer), the efficiency of the overall circuit can be high. However, the efficiency is generally a function of output current and typically decreases at low output current. This reduction in efficiency is generally attributable to the losses

associated with operating the switching regulator. These losses include, among others, quiescent current losses in the control circuitry of the regulator, switch losses, switch driver current losses and inductor/transformer winding and core losses.

The reduction in efficiency of a switching regulator at low output current can become important in battery-operated systems where maximizing battery lifetime is desirable.

In view of the foregoing, it would be desirable to provide a high efficiency switching regulator.

It would also be desireable to provide a control circuit and method for maintaining high efficiency over broad current ranges, including low output currents, in a switching regulator circuit.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a high efficiency switching regulator.

It is also an object of the present invention to provide a control circuit and method for maintaining high efficiency over broad current ranges, including low output currents, in a switching regulator circuit.

In accordance with these and other objects of the invention, there is provided a circuit and method for controlling a switching voltage regulator having (1) a switch including one or more switching transistors and (2) an output adapted to supply current at a regulated voltage to a load including an output capacitor. The circuit and method generates a control signal to turn the one or more switching transistors OFF under operating conditions when the voltage at the output is capable of being maintained substantially at the regulated voltage by the charge on the output capacitor (e.g., during low output currents). During such periods of time, the load does not consume power from the input power source. Therefore, the regulator efficiency is increased. If desired, other components in the switching regulator, in addition to switching transistors, can also be intentionally held OFF to conserve additional power. This additional feature of the present invention can further increase the efficiency of the overall regulator circuit.

The circuit and method of the present invention can be used to control various types of switches in switching regulator circuits, including switches that use either one or more power transistors. Additionally, the circuit and method can be used to control switches in various types of switching regulator configurations, including voltage step-down, voltage step-up and polarity-inversing configurations.

Additionally, the circuit and method of the present invention can vary the OFF time of the switching transistor in response to the input and output voltages of the switching regulator. This feature of the present invention reduces the emission of audible noise from the switching regulator during low input voltage conditions. It also reduces the potential for current runaway during short circuits in the output voltage for some regulator configurations.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the present invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. 1 is a schematic block diagram of a typical prior art switching regulator circuit employing a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 2 is a schematic block diagram of a switching regulator circuit incorporating a first embodiment of the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 3 is a schematic block diagram of a switching regulator circuit incorporating a second embodiment of the high-efficiency control circuit of the present invention to drive a switch including a switching MOSFET and a switching diode in a step-down configuration;

FIG. 4 is a schematic block diagram of a switching regulator circuit incorporating a "user-activated" embodiment of the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 5 is a schematic block diagram of a switching regulator circuit incorporating the variable OFF-time control circuit of the present invention;

FIG. 6 is a detailed schematic diagram of an embodiment of the variable OFF-time control circuit of FIG. 5;

FIG. 7 is a detailed schematic block diagram of an exemplary switching regulator circuit incorporating both the variable OFF-time feature and the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 8 is a schematic block diagram of a switching regulator circuit incorporating a circuit of the present invention for preventing reversals in the polarity of the current in the output inductor of the regulator from drawing power from the load;

FIG. 9 is a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a step-up configuration; and

FIG. 10 is a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a polarity-reversing configuration.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic block diagram of a typical prior art switching regulator circuit employing a push-pull switch in a step-down configuration.

Referring to FIG. 1, circuit 10 is used to provide a regulated DC output voltage V_{OUT} at terminal 12 (e.g., 5 volts) for driving load 14 which, for example, may be a portable or laptop computer or other battery-operated system. Circuit 10 operates from an unregulated supply voltage V_{IN} coupled to terminal 14 (e.g., a 12 volt battery). Circuit 10 includes push-pull switch 15, driver circuit 20, output circuit 30 and control circuit 35.

Driver circuit 20 is used to drive push-pull switch 15 which includes two synchronously-switched power MOSFETS 16 (p-channel) and 17 (n-channel) stacked in series between supply rail V_{IN} and ground. Push-pull switch 15 in conjunction with driver circuit 20 is typically referred to as a "half-bridge" configuration. MOSFETS 16 and 17 are used to alternately supply current to output circuit 30 which includes inductor 32 (L1) and output capacitor 34 (C_{OUT}). Output circuit 30 smooths the alternating supply of current so that load 12 is provided a regulated voltage V_{OUT}. In order to supply the alternating current, MOSFETS 16 and 17 are respectively driven by P-channel driver 26 and N-channel driver 27, which in turn are both controlled by control circuit 35.

Control circuit 35 includes one-shot circuit 25 which provides an OFF pulse of constant duration (e.g., 2 to 10 microseconds) during which time MOSFET 16 is held OFF and MOSFET 17 is held ON by drivers 26 and 27, respectively. Otherwise, one-shot circuit 25 provides an ON pulse during which time MOSFET 16 is held ON and MOSFET 17 is held OFF. Therefore, one-shot circuit 25 alternately turns MOSFETS 16 and 17 ON and OFF to provide an alternating supply of current to (output circuit 30. The duty cycle of the one-shot circuit 35 is in turn controlled by current amplifier 39.

Control circuit 35 monitors the output voltage V_{OUT} through resistor-divider network R_1/R_2 (36A/36B) to provide a feedback voltage V_{FB} proportional to the output voltage V_{OUT}. Control circuit 35 also monitors the current I_L through inductor L1 to provide a feedback current I_{FB} proportional to inductor current I_L. Circuit 10 operates by controlling inductor current I_L so that the feedback voltage V_{FB} is regulated to be substantially equal to a reference voltage V_{REF} provided by reference circuit 37. With feedback voltage V_{FB} being regulated, the output voltage V_{OUT} is in turn regulated to a higher voltage by the ratio of (R_1+R_2) to R_2.

Transconductance amplifier 38 is used to compare the feedback voltage V_{FB} to a reference voltage V_{REF}. Circuit 10 regulates the output voltage V_{OUT} as follows. During each cycle when switch 15 is "ON", P-MOSFET 16 is turned ON and the current I_L in inductor L1 ramps up at a rate dependent on $V_{IN}-V_{OUT}$. When I_L ramps up to a threshold level set by output 38A of transconductance amplifier 38, current comparator 39 trips and triggers the one-shot OFF pulse, initiating the "OFF" cycle of switch 15. During the "OFF" cycle, one-shot circuit 25 holds P-MOSFET 16 OFF and turns N-MOSFET 17 ON. This in turn causes the current I_L in inductor L1 to ramp down at a rate dependent on V_{OUT}. Thus, the duty cycle of the periodic turning OFF of switch 15 is controlled so the current I_L produces a regulated output voltage V_{OUT} at terminal 12.

As the output load current increases, the voltage drop across R_2 resistor 36B will decrease. This translates into a small error voltage at input 38B of transconductance amplifier 38 that will cause output 38A to increase, thus setting a higher threshold for current comparator 39. Consequently, current I_L in inductor L1 is increased to the level required to support the load current.

Since the OFF time (t_{OFF}) of one-shot circuit 25 is constant, switching regulator circuit 10 has a constant ripple current in inductor L1 (for constant output voltage V_{OUT}), but has a frequency which varies with V_{IN}. The ripple oscillation frequency is given by the equation:

$$f_{RIP}=(1/t_{OFF})\ [1-(V_{OUT}/V_{IN})]$$

One disadvantage of circuit 10 in FIG. 1 is that the ripple oscillation frequency f_{RIP} may decrease to an audible level with low input voltages V_{IN}. This could occur, for example, when a battery powering the switching regulator circuit is nearly discharged. Inductor L1 may then generate and emit noise that can be objectionable to a user of the device employing the regulator circuit.

An additional disadvantage of prior art circuit **10** is that the inductor current I_L is not well controlled when the output voltage V_{OUT} is shorted to ground. The basic relationship between inductor current and voltage is given by the equation di/dt=V/L. This means that the rate at which current I_L in inductor L1 decays during the OFF-time depends on the voltage across inductor L1, which is the sum of V_{OUT} and the drain to source voltage, V_{DS}, of N-MOSFET **17**. During a short, V_{OUT} approaches zero while V_{DS} is also very low, resulting in very little decay of current I_L in inductor L1 during t_{OFF}. However, following each OFF cycle, P-MOSFET **16** is turned back ON until current comparator **39** again trips one-shot constant OFF time control circuit **25**. Even for the minimum time that P-MOSFET **16** is ON, the current I_L in inductor L1 may increase by more than it can decrease during t_{OFF}. This may result in a runaway condition in which the short circuit current may reach destructive levels.

A further disadvantage of prior art circuit **10** results from the constant ripple current in inductor L1. During t_{OFF}, current I_L in inductor L1 always ramps down by the same amount regardless of the output current of the regulator. At low output currents this can cause the current in inductor L1 to reverse polarity and, thus, pull power from the load. During the following ON cycle, this current again ramps positive such that the average inductor current equals the load current. Losses associated with this constant ripple current, along with switching losses due to the charging and discharging of switch **15**'s MOSFET gates, can produce large reductions in efficiency at low output currents. This will be especially the case if the current in inductor L1 reverses and power is pulled from the load to ground through N-MOSFET **17**.

A still further disadvantage of prior art circuit **10** concerns the gate drives to P-MOSFET **16** and N-MOSFET **17**. Delays are generally incorporated into drivers **26** and **27** to ensure that one power MOSFET turns OFF before the other turns ON. If there is insufficient deadtime between the conduction of the two MOSFETs (due to, for example, device, circuit processing, or temperature variations), current will be passed directly from input supply V_{IN} to ground. This "shoot-through" effect can dramatically reduce efficiency, and in some circumstances, can overheat and destroy the power MOSFETs.

FIG. **2** is a schematic block diagram of a switching regulator circuit incorporating a first embodiment of the high-efficiency control circuit of the present invention for driving a switch including a pair of synchronously-switched MOSFETs in a step-down configuration.

Switching regulator circuit **50** includes push-pull switch **15**, driver circuit **20** and output circuit **30** similar to those of FIG. **1**. Circuit **50** also includes an embodiment **70** of the high-efficiency control circuit of the present invention.

Control circuit **70** includes one-shot circuit **25**, current comparator **39** and amplifier **38** similar to those of FIG. **1**. However, in addition to those components, control circuit **70** also includes constant current source I_1 **72** and hysteretic comparator **74** for providing high efficiency operation at low average current levels.

As will be discussed in greater detail below, constant current source I_1 **72** and comparator **74** allow push-pull switch **15** to go into a state of operation where both MOSFETS **16** and **17** are simultaneously OFF under conditions where the output voltage V_{OUT} can be maintained substantially at the regulated voltage V_{REG} by output capacitor C_{OUT}. This state of operation is referred to herein as a "sleep mode." The ability of push-pull switch **15** to go into such a sleep mode is in contrast to the regulator circuit of

FIG. **1** where one of the two MOSFETs **16** and **17** is substantially ON at all times. This feature of the present invention reduces the regulator circuit power consumption since push-pull switch **15** does not dissipate power or allow power to be pulled from load R_L to ground in sleep mode.

Furthermore, if desired, while push-pull switch **15** is in the above-described sleep mode, the regulator circuit can turn OFF other circuit components which are not needed while the regulator is in sleep mode. For example, for the embodiment of the present invention shown in FIG. **2**, one-shot circuit **25**, current comparator **39**, current source I_1 **72** and amplifier **38** can also be turned OFF in sleep mode. This feature of the present invention allows the regulator circuit to operate at even higher efficiencies than otherwise possible if only push-pull switch **15** were maintained in a sleep mode.

At high load current levels (e.g., greater than 20 percent of the maximum rated output current) control circuit **70** operates similar to control circuit **35** of FIG. **1**. In FIG. **2**, the current feedback I_{FB} is again provided to the non-inverting input of current comparator **39**. Offset V_{OS} **76**, which preferably is built into amplifier **38**, level-shifts feedback voltage V_{FB} slightly below reference voltage V_{REF}, thus keeping the output of hysteretic comparator **74** high during high current conditions. When the feedback current I_{FB} exceeds the current supplied to the inverting input of current comparator **39**, the output of comparator **39** goes HIGH so as to initiate the switch "OFF" cycle.

During the "OFF" cycle, output **25A** of one-shot circuit **25** is HIGH, which turns P-MOSFET **16** OFF and N-MOSFET **17** ON. After a constant time set by one-shot circuit **25**, output **25A** goes LOW, thus initiating the next "ON" cycle where P-MOSFET **16** ON and N-MOSFET **17** OFF.

In accordance with the present invention, regulator circuit **50** goes into sleep mode at low output current levels as follows. Hysteretic comparator **74** monitors the feedback voltage V_{FB} and goes LOW when V_{FB} exceeds a predetermined voltage value in excess of the reference voltage V_{REF}. Such a condition is indicative of the output voltage V_{OUT} exceeding a predetermined voltage value in excess of the regulated voltage V_{REG}. This over voltage condition is intentionally induced at low average output currents by providing a constant current source I_1 **72** coupled in parallel with amplifier **38**. During the over voltage condition both MOSFETS **16** and **17** are maintained OFF by way of AND gate **66** and NAND gate **68**.

Constant current source I_1 sets a minimum feedback current threshold for current comparator **39**. This sets a minimum current required in inductor L1 during each ON cycle to trip comparator **39**. In accordance with the present invention, current comparator **39** is intentionally forced to remain ON at current levels that would otherwise cause it to trip. Thus, more current is supplied to inductor L1 than is necessary to maintain the output voltage V_{OUT} at the regulated voltage V_{REG}. As a result, V_{OUT} will begin to increase beyond the regulated voltage V_{REG}, causing the feedback voltage V_{FB} to trip hysteretic comparator **74** at a predetermined voltage value in excess of V_{REF}. When comparator **74** trips, its output goes LOW to turn both MOSFET **16** and **17** OFF to put the regulator circuit into sleep mode.

In the above-described state of operation (i e., "sleep mode") where MOSFETs **16** and **17** are both simultaneously OFF, the output load **14** is supported substantially by output capacitor C_{OUT}. Hysteretic comparator **74** monitors the feedback voltage V_{FB} and when V_{OUT} falls such that V_{FB} has decreased by the amount of the hysteresis in comparator **74**, driver circuit **20** is taken out of sleep mode (where

MOSFETS **16** and **17** are both driven OFF) so that a new ON cycle is initiated to supply current to load **14**. If the load current remains low, C_{OUT} will recharge to a voltage level in excess of V_{REG} and the feedback voltage V_{FB} will again trip comparator **74** after only a few cycles.

Thus, during light loads, control circuit **70** is adapted to turn both MOSFET **16** and MOSFET **17** OFF when they are not needed to maintain the output voltage substantially at the regulated voltage level if the output capacitor C_{OUT} is capable of doing so. When the output voltage falls below the regulated voltage level in such a mode, control circuit **70** is adapted to briefly turn switch **15** ON to recharge the output capacitor C_{OUT} back to a voltage level in excess of the regulated voltage. Therefore, V_{OUT} will oscillate between upper and lower thresholds separated by the comparator **74** hysteresis voltage multiplied by the ratio of (R_1+R_2) to R_2. The rate at which the regulator "wakes up" to recharge output capacitor C_{OUT} will automatically adapt to the load current, maintaining high efficiencies even at low output currents.

In accordance with the present invention, control circuit **70** maintains MOSFETS **16** and **17** OFF over periods of time when the output current is low enough to allow the output capacitor C_{OUT} to maintain the output voltage substantially at the regulated voltage. Typically, such periods of OFF time, wherein both MOSFETS **16** and **17** are maintained OFF even though the switching regulator is providing a regulated voltage, can extend from less than 100 microseconds to over a few seconds (respectively corresponding to a few switch cycles to over one-hundred-thousand switch cycles for a switching frequency of 100 kilohertz). Such OFF times typically allow high efficiency to be obtained (e.g., over 90%) over an output current range in excess of 100:1. Because other components in addition the switching transistors can also be maintained OFF during such periods, even higher efficiencies can typically be obtained.

Control circuit **70** of switching regulator **50** shown in FIG. **2** is used to drive a synchronously-switched switch including MOSFETs **16** and **17**. As used herein, the term "synchronously-switched switch" refers to a switch including two switching transistors that are driven out of phase to supply current at a regulated voltage to a load. FIG. **3** shows a second embodiment of the high-efficiency control circuit of the present invention adapted to drive a switch including a switching transistor and a switching diode in a step-down configuration.

As shown in FIG. **3**, switching regulator circuit **100** includes switch **115** including P-MOSFET **116** and diode **118**. Switch **115** is driven by driver **120** including P-driver **126**. The turning-ON and turning-OFF of switch **115** is controlled by control circuit **125**. Because control circuit **125** is used to only drive one MOSFET (in contrast to control circuit **70** of FIG. **2**), it only has one output terminal **125**A (taken from the output of NAND gate **68**).

Control circuit **125** includes current comparator **39**, amplifier **38**, hysteretic comparator **74** and one-shot circuit **25**, similar to those shown in control circuit **70** of FIG. **2**. As discussed above with respect to FIG. **2**, at low average output current levels, constant current source I_1 **72** is used to intentionally overdrive the current supplied to inductor L1 so as to cause the output voltage V_{OUT} to increase beyond the regulated voltage level V_{REG} where the output can be supported substantially by output capacitor C_{OUT} for extended periods of time. During these extended time periods, P-MOSFET **116** is maintained OFF in a sleep mode so as to increase circuit efficiency.

As discussed above, control circuits **70** and **125** of FIGS. **2** and **3**, respectively, provide high-efficiency operation at low average output current levels. Such operation adapts automatically to the output current level. For example, at high output current levels during a first state of operation the switch continually alternates between an ON state and an OFF state to maintain the output voltage V_{OUT} at the regulated voltage level V_{REG}. At low output current levels during a second state of operation, where circuit efficiency would otherwise be low, the output voltage V_{OUT} is able to be maintained substantially at the regulated voltage level V_{REG} by output capacitor C_{OUT} without continuously turning the switch ON and OFF. Thus, the control circuit automatically identifies such a condition and allows the regulator circuit to go into a "sleep" mode where a minimal number of circuit components are required to be ON.

In accordance with another feature of the present invention, a regulator circuit can also incorporate a "user activated" embodiment of the control circuit of the present invention where a user input controls whether the regulator circuit is in a "sleep" mode or not. FIG. **4** is a schematic block diagram of a switching regulator circuit incorporating such a "user-activated" embodiment of the high-efficiency control circuit of the present invention for driving a switch including a pair of synchronously-switched MOSFETs in a step-down configuration.

Switching regulator circuit **150** in FIG. **4** includes push-pull switch **15**, driver **20**, output circuit **30** similar to those in circuit **50** of FIG. **2**. Control circuit **170** of regulator circuit **150** includes one-shot circuit **25**, current comparator **39** and amplifier **38** also similar to those in circuit **50** of FIG. **2**. In contrast to FIG. **2**, switch **175** (including switches **176** and **178**) is used to manually switch regulator circuit **150** into a sleep mode through user input **175**A, which may be a control signal from some other type of control circuit (not shown). Upon the closing of switch **175**, switches **176** and **178** both close.

Switch **176** is used to turn N-driver **27** OFF in sleep mode by grounding input **66**A of AND gate **66** (which normally is held HIGH by resistor **67** coupled to a positive supply). Switch **178** is used to introduce positive feedback, and therefore hysteresis, into amplifier **38** so as to allow control circuit **170** to maintain the output voltage V_{OUT} substantially at the regulated voltage level V_{REG} in sleep mode. (Resistor R_{HYS}, coupled between reference circuit **37** and the non-inverting input of transconductance amplifier **38**, is used to assist in feeding back the output of amplifier **38** into the non-inverting input of amplifier **38**.)

Switch **178** allows amplifier **38** to overdrive the supply of current to inductor L1 (through P-MOSFET **16**) so as to intentionally drive the output voltage V_{OUT} to a predetermined level in excess of the regulated voltage level V_{REG}. After being driven to such voltage level, the hysteresis in amplifier **38** maintains P-driver **26** OFF until the feedback voltage V_{FB} falls by at least the hysteresis voltage. At that point, output **39**A of current amplifier **39** goes HIGH to trigger one-shot circuit **25** so that P-MOSFET **16** is turned ON to re-charge the output capacitor C_{OUT} to the predetermined voltage level in excess of the regulated voltage level V_{REG}.

AS discussed above, control circuit **170** periodically wakes up during sleep mode to turn P-MOSFET **16** ON to recharge the output capacitor C_{OUT}. It will be apparent to those of ordinary skill in art that although N-MOSFET **15** is maintained OFF during such wake-up periods, this does not have to be the case. For example, while control circuit **170** is recharging output capacitor C_{OUT}, such recharging could

be accomplished by alternately turning the switching transistors OFF so as to vary the duty cycle and thereby recharge the output capacitor C_{OUT}.

Thus, regulator circuit **150** operates to increase efficiency at low current levels as in regulator circuit **50** of FIG. **2** if a user manually activates a switch. However, in contrast to regulator circuit **50** of FIG. **2**, regulator circuit **150** does not automatically adapt to the output current levels. For example, circuit **150** does not take itself out of sleep mode as the average output current increases—it relies upon user deactivation.

As discussed above, the embodiments of the control circuits of the present invention shown in FIGS. **2–4** include one-shot circuit **25**. In accordance with another feature of the present invention, the one-shot circuit could be replaced with other types of circuits that control the duty cycle of the power switch. For example, one-shot circuit **25** could be replaced with a pulse-width modulator circuit that provides a pulse-width modulated signal in response to a control signal. Of course, other types of circuits could be used as well.

In accordance with another feature of the present invention, one-shot circuit **25**, which provides a constant OFF-time signal, could be replaced with a one-shot circuit that provides a variable OFF-time control signal dependent upon the output voltage (V_{OUT}) and the input voltage (V_{IN}). This feature of the present invention can be used to reduce the generation and emission of audible noise from inductor L1 at low input voltages. As discussed above, such noise is associated with oscillation in the inductor current. Furthermore, this feature of the present invention can also be used to control the short circuit current if the output is short circuited.

FIG. **5** is a schematic block diagram of an exemplary switching regulator circuit incorporating the variable OFF-time control circuit of the present invention.

Switching regulator circuit **200** includes push-pull switch **15**, driver circuit **20**, current feedback circuit **210**, voltage feedback circuit **220**, feedback control circuit **230** and variable OFF-time circuit **240**. Feedback control circuit **230** monitors the output current and output voltage through inputs **232** and **234**, respectively, and provides a trigger signal at terminal **236** to initiate the OFF cycle of switch **15**. Variable OFF-time circuit **240** is used to control the OFF time as follows.

Circuit **240** includes one-shot generator **245** which is triggered by feedback control circuit **230** through terminal **236**. One-shot generator **245** includes an additional terminal **245A** coupled to control capacitor (C_{CON}) **246** whose voltage is monitored by generator **245**. In accordance with the present invention, OFF-time control circuit **250** controls the discharging of capacitor C_{CON}, and thus the capacitor voltage, so as to in turn control the OFF time of generator **245**. OFF-time control circuit **250** monitors the input and output voltages (V_{IN} and V_{OUT}) and, depending upon their values, adjusts the OFF time accordingly.

In accordance with the present invention, if the input voltage V_{IN}, decreases so that the inductor L1 oscillation frequency f_{RIP} discussed above falls into an audible range, the OFF time is decreased so that f_{RIP} will accordingly increase out of an audible range. Also, if the output voltage V_{OUT} decreases due to a short circuit so that the voltage across inductor L1 is too low to allow adequate decay in inductor current during the OFF cycle, the OFF time is increased so as to avoid a current runaway condition.

In the present embodiment the discharging of control capacitor C_{CON} is regulated by controlling the magnitude of control current I_{CON}. For example, at low input voltages I_{CON} is increased by OFF-time control circuit **250** so that the voltage on control capacitor C_{CON} rapidly falls. When the control capacitor voltage falls below a predetermined value, the ON cycle of switch **15** is initiated. Additionally, at low output voltages I_{CON} is decreased by OFF-time control circuit **250** so that the voltage on control capacitor C_{CON} slowly decays to lengthen the OFF time.

Although switching regulator circuit **200** shown in FIG. **5** relies upon a particular circuit for discharging a capacitor to control the OFF time, it is apparent that other circuits for performing this same function in response to the input and output voltages can also be used. For example, if desired, an operational amplifier could be used to control the OFF-time.

Thus, a one-shot circuit has been discussed which provides a variable OFF-time control signal that adapts to the input and output voltage levels. This feature of the present invention is used to reduce the generation and emission of audible noise from the regulator circuit at low input voltage levels (i.e., reduce t_{OFF} at low input voltages) and to limit the short circuit current if the output is short circuited (i.e., increase t_{OFF} at low output voltages).

FIG. **6** is a detailed schematic diagram of an exemplary embodiment of the variable OFF-time control circuit of FIG. **5**.

OFF-time control circuit **250** accepts as inputs V_{IN} and V_{OUT} at terminals **252** and **254**, respectively, and provides an output I_{CON} at terminal **256**. As discussed above, I_{CON} provides for the controlled discharging of a control capacitor C_{CON} coupled to terminal **256**. Control circuit **250** controls the magnitude of I_{CON}, and therefore controls the time it takes control capacitor C_{CON} to discharge. Control circuit **250** includes current source **260** (for providing current I_{CN2}), current source **270** (for providing current I_{CN1}), current compensation circuit **280** and current mirror output circuit **295**. Control circuit **250** works as follows.

Current mirror output circuit **295** is a current mirror circuit including transistor **296** and transistor **298** (having its gate **298A** connected to its drain **298B**). Circuit **295** accepts a controlled reference current I_{CREF} at input **295A** and provides a proportional output current I_{CON} related to the aspect ratios of transistor **296** and **298** (as in conventional current mirror circuits). In accordance with the present invention, I_{CREF} will be equal to either I_{CN1} or ($I_{CN1}+I_{CN2}$) depending upon voltages V_{IN} and V_{OUT} on input terminals **252** and **254**, respectively.

When $V_{IN}-V_{OUT}$ is greater than 1.5volts, transistor **262** conducts sufficient current (from transistor **264** and current supply I_6) to hold transistor **266** OFF. With transistor **266** OFF, current I_{CN2} will be zero and current I_{CREF} will therefore be equal to current C_{CN1} provided at output terminal **270A** of current source **270**.

Current I_{Cn1} is supplied by a current mirror circuit composed of transistor **272** and transistor **274** (having its gate **274A** connected to its drain **274B**). In accordance with the present invention, the reference current I_{CN1REF} flowing from transistor **274** will be equal to either I_{CN1A} or ($I_{CN1A}+I_{CN1B}$), depending upon whether transmission gate **282** is open or closed, respectively.

Transmission gate **282** is controlled by comparator **284** and will be OPEN when V_{OUT} is less than V_{TH3}. Under OPEN conditions, I_{CN1REF} will be equal to I_{CN1A} which goes to the collector of transistor **276**. This current is derived by dividing V_{OUT} by the output divider (composed of resistors **271** and **273**) to produce voltage V_{FB1} (at the base of

transistor **279**). Voltage V_{FB1} is then level shifted up by the base-emitter voltage of transistor **279** and then down by the base-emitter voltage of transistor **276** where it appears across emitter resistor **278**. The resulting transistor **276** collector current is then proportional to the output voltage V_{OUT}, causing control capacitor C_{CON} to be discharged at a rate which is proportional to the discharge rate of the current in inductor L1.

Thus, when the output voltage V_{OUT} is low, such as during a fault or start-up condition, t_{OFF} will be lengthened to allow the additional time required for the current to ramp down in inductor L1.

When the output voltage V_{OUT} is greater than V_{TH3}, the output of comparator **284** closes transmission gate **282** to couple an additional compensation current I_{CN1B} is to the drain of transistor **274** to provide current compensation through current compensation circuit **280**. Compensation current I_{CN1B} is equal to current I_{TRIM} minus the drain current of transistor **286**. Transistors **286** and **288** serve to mirror the collector current in transistor **290** (which is derived in a similar manner to the collector current in transistor **276** discussed above, except that voltage V_{REF} is used instead of voltage V_{FB1}).

Compensation current I_{CN1B} has two purposes: 1) to serve as a trimming current to set a desired control current I_{CON} when the output voltage V_{OUT} is substantially at its regulated level, and 2) to maintain a substantially constant control current I_{CON} over a wide range of operating temperatures. During typical circuit manufacturing, variations in the resistance of resistor **278** would normally cause control current I_{CON} to be larger or smaller than desired. By trimming I_{TRIM} while in production, compensation current I_{CN1B} can be adjusted to add or subtract from the collector current (I_{CN1A}) of transistor **276** as required to provide a predetermined control current I_{CON}. Additionally, if resistors **278** and **292** are matched (i.e., designed and fabricated similarly), then control current I_{CON} variations due to the temperature variation of the resistance of resistor **278** will be substantially cancelled by a corresponding change in the resistance of resistor **292**.

If the output voltage V_{OUT} is less than voltage V_{TH3}, the output of comparator **284** opens transmission gate **282** and thus inhibits current compensation. This ensures that control current I_{CON} will approach zero as the output voltage V_{OUT} approaches zero, thus guaranteeing control of the inductor current I_L during an output short circuit.

When V_{IN} falls to the point that $V_{IN}-V_{OUT}$ is less than 1.5 volts, the current in transistor **262** no longer holds transistor **266** OFF. As V_{IN} decreases further, transistor **266** adds additional current (I_{CN2}) into current mirror output circuit **295**, thereby increasing control current I_{CON} and, thus, reducing t_{OFF}. This in turn stabilizes the operating frequency as V_{IN} decreases, reducing potential audibility problems. Current source I_7 determines the maximum current that transistor **266** adds to control current I_{CON}.

Thus, when V_{IN} falls so that $V_{IN}-V_{OUT}$ is less than 1.5 volts (e.g., when a battery is nearly discharged), t_{OFF} will be reduced to increase the oscillation frequency of the regulator circuit so that the generation and emission of audible noise is reduced.

Although variable OFF-time control circuit **250** was discussed above with respect to a regulator circuit which includes push-pull switch **15** and driver **20**, it will be apparent that the variable OFF-time feature of the present invention could be used in other regulators as well. For example, this feature could also be used in the regulator circuits of FIGS. **3** and **4** and other circuits that employ one-shot generators to provide a regulated voltage.

FIG. **7** is a detailed schematic block diagram of an exemplary switching regulator circuit incorporating both the variable OFF-time feature and the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration.

Switching regulator **300** includes push-pull switch **15**, driver **20**, output circuit **30** and control circuit **350**. Control circuit **350** includes one-shot generator **245**, variable OFF-time control circuit **250** for controlling the OFF cycle time and comparator **74** for providing high-efficiency operation at low average output current levels. Switching regulator **300** works as follows.

When the load current exceeds, for example, approximately 20 percent of the maximum output current, the loop operates in a continuous mode wherein comparator **74** does not override output **245A** of one-shot generator **245**. With $V_{IN}-V_{OUT}$ greater than 1.5 V, operation is substantially similar to that described for FIG. **1**. The inductor current is sensed by means of the voltage drop across resistor R_{SENSE}, and the threshold for the current comparator **39** is set by the voltage drop across resistor R_3. Built-in offset V_{OS} (e.g., about 10 mv) levelshifts feedback voltage V_{FB} slightly below reference voltage V_{REF}, thus keeping the output of comparator **74** HIGH in this mode. When the voltage across resistor R_{SENSE} exceeds the threshold across resistor R_3, the output of comparator **39** goes HIGH and the RBAR input of RS flip-flop **310** goes LOW, resetting RS flip-flop **310**, and thus, initiating the switch OFF cycle.

During the OFF cycle, switch signal V_{SWB} is HIGH, which turns P-MOSFET **16** OFF, N-MOSFET **17** ON and allows I_{CON} to discharge control capacitor C_{CON}. The OFF time, t_{OFF}, is in turn determined by the time it takes control capacitor C_{CON} to discharge from its initial voltage to V_{TH1}, coupled to the non-inverting input of comparator **312**. When control capacitor C_{CON} discharges to voltage V_{TH1}, the output of comparator **312** goes LOW, thus setting RS flip-flop **310** and initiating the next ON cycle. Voltage V_{TH1} is higher than voltage V_{TH2}, thus causing the output of comparator **315** to remain LOW in the continuous mode.

In accordance with present embodiment, the OFF time is controlled by variable OFF-time control circuit **250** described above with respect to FIGS. **5** and **6**. Accordingly, circuit **250** includes inputs **252** and **254** coupled to V_{IN} and V_{OUT}, respectively, to monitor those voltages.

current source I_1 sets a minimum voltage threshold across resistor R_3 for current comparator **39**. This sets a minimum current required in inductor L1 during each ON cycle to trip comparator **39**. If the resulting average inductor current flowing to the output is greater than the load current, then output voltage V_{OUT} will begin to increase, causing feedback voltage V_{FB} to trip the hysteretic comparator **74**. Of course, the inductance of inductor L1 and OFF time t_{OFF} are preferably chosen so that the inductor ripple current is not below zero when such tripping occurs. When comparator **74** trips, its output goes LOW and overrides the Q output of RS flip-flop **310**, immediately switching switch signal V_{SWB} high. As discussed above, this automatically initiates the beginning of the "sleep" mode of operation.

In sleep mode, capacitor C_{CON} discharges as before, but does not initiate a new switch ON cycle when comparator **312** trips. As discussed above, this is because until feedback voltage V_{FB} has fallen by the amount of hysteresis in comparator **74**, the LOW at output **74A** forces switch signal V_{SWB} to remain HIGH through NAND gate **316**. Accordingly, control capacitor C_{CON} continues to discharge below voltage V_{TH2}, causing output **315A** of comparator **315** to go

HIGH. This in turn causes the N-MOSFET **17** as well as the P-MOSFET **16** to be turned OFF. In addition, unused circuit components such as amplifier **38** and comparators **39** and **312** are also turned OFF when the regulator circuit is in sleep mode. As discussed above, this decreases bias currents substantially during sleep mode, further increasing efficiency at low output current levels.

During the extended off times in sleep mode, much of the regulator and both MOSFETS **16** and **17** are turned off, and the output load is supported substantially by output capacitor C_{OUT}. However, when the output voltage V_{OUT} falls such that the feedback voltage V_{FB} has decreased by the amount of hysteresis in comparator **74**, all circuit components are again turned on and a new ON cycle is initiated to supply current to the output. If the load current remains low, output capacitor C_{OUT} will recharge, and the feedback voltage V_{FB} will again trip comparator **74** after only a few switch cycles. Thus, during light load conditions, the output voltage V_{OUT} will oscillate between upper and lower thresholds values, as discussed above.

Whenever P-MOSFET **16** is ON, its gate-to-source voltage also appears across MOSFET **334**, turning MOSFET **334** ON. This pulls the drain of MOSFET **334** HIGH, and inhibits N-drive **27**. Following a LOW-to-HIGH V_{SWB} transition, the voltage on the gate of P-MOSFET **16** must rise to a level where MOSFET **334** is conducting less than current source **335** before the drain voltage of MOSFET **334** falls and allows the N-MOSFET **17** to be turned ON. Current I_{M1} is purposely made small so that the gate of MOSFET **334** must rise to within **2** volts of the input voltage V_{IN} before the drive is enabled, ensuring that the P-MOSFET is completely OFF when N-MOSFET **17** turns ON. In a similar manner, MOSFET **332** and current source I_{M2} **333** ensure that the N-MOSFET **17** is completely OFF when the P-MOSFET **16** turns ON. This prevents simultaneous conduction regardless of the driver speeds or MOSFET sizes, ensuring maximum possible efficiency. This feature of the present embodiment is discussed in more detail in commonly-assigned U.S. patent application Ser. No. 07/893,523, filed Jun. 4, 1992, now U.S. Pat. No. 5,365,118, which is hereby incorporated by reference in its entirety. If desired, the control circuit of the present invention can also include circuitry for accommodating transient switch signals as described in copending commonly-assigned U.S. patent application Ser. No. 08/035,423, filed concurrently herewith , now U.S. Pat. No. 5,408,150, which is also hereby incorporated by reference in its entirety.

Schottky diode D**2** coupled across N-MOSFET **17** shown in FIG. **7** only conducts during the deadtime between the conduction of MOSFETS **16** and **17**. Diode D2's purpose is to prevent the body diode of N-MOSFET **17** from turning on and storing charge during the deadtime, which could reduce efficiency (e.g., by approximately 1 percent) in some cases. Diode D2 preferably is selected with a forward voltage of less than about 0.5 volts when conducting the maximum output current.

In accordance with the present invention, the control circuit shown in FIG.7, when incorporated into a 5-volt synchronous step-down switching regulator, is capable of achieving over 90 percent efficiency (for an input voltage of approximately 10 volts) while the output current varies over two orders of magnitude (e.g., 20 mA to 2 A). Under some operating conditions (e.g., for an input voltage of 6 volts) efficiencies of over 95 percent can be maintained over such current levels. Such a control circuit is particularly useful in notebook and palm-top computers, portable instruments, battery-operated digital devices, cellular telephones, DC power distributions systems and GPS systems.

As discussed above with respect to FIG. **1**, a disadvantage of prior art control circuit **10** is that at low output currents the current in inductor L**1** may reverse polarity if during t_{OFF} the current ramps down too much. This may result in power being pulled from the load to ground, through N-MOSFET **17**, with an associated reduction in circuit efficiency. In accordance with a still further feature of the present invention, the control circuit can include a circuit for turning OFF the N-MOSFET to prevent such power from being pulled from the load if the inductor current reverses polarity.

FIG. **8** is a schematic block diagram of an exemplary switching regulator circuit incorporating a circuit of the present invention for preventing reversals in the polarity of the current in the output inductor of the regulator from drawing power from the load.

Switching regulator **400** includes push-pull switch **15**, driver circuit **20** and output circuit **30** similar to those of FIG. **1**. Circuit **400** also includes an embodiment **470** of the high-efficiency control circuit of the present invention for preventing reversals in the polarity of output inductor L1 current from drawing power from the load.

Control circuit **470** includes one-shot circuit **25**, current comparator **39** and transconductance amplifier **38** similar to those of FIG. **1**. In addition to those components, control circuit **470** also includes comparator **471** and gate **472** for preventing reversals in inductor current polarity from drawing power from the load at low average current levels. Control circuit **470** works as follows.

When output **25***a* of one-shot circuit goes HIGH to turn P-MOSFET **16** OFF and N-MOSFET **17** ON, the inductor current I_L begins to ramp down. During low average output currents, this current may ramp down towards zero and, eventually, may go negative. Control circuit **470** works by monitoring the inductor current I_L, through current feedback signal I_{FB2}, and turns N-MOSFET **17** OFF before such current reversals can occur. This prevents N-MOSFET **17** from drawing power from the load to ground.

Comparator **471** includes an input **471***a* adapted to monitor inductor current I_L by way of current feedback signal I_{FB2}. When current feedback signal I_{FB2} falls below current I_4 applied to input **471***b* of comparator **471**, comparator output **471***c* goes LOW and, therefore, turns N-MOSFET **17** OFF by way of NAND gate **472**. The turning OFF of N-MOSFET **17** prevents current reversals in inductor current I_L from drawing power from load **14** to ground through N-MOSFET **17**.

After N-MOSFET **17** is turned OFF, it will again be allowed to turn ON as soon as feedback current I_{FB2} exceeds current I_4 to cause comparator output **471***c* to go HIGH. Generally, comparator output **471***c* will again go HIGH after one-shot circuit **25** turns P-MOSFET **16** ON, which, in turn, causes the inductor current I_L to again ramp up. Such ramping up will allow current feedback signal I_{FB2} to exceed I_4 and, therefore, cause comparator output **471***c* to go HIGH. While comparator **471***c* is HIGH, one-shot circuit **25** solely controls the turning ON of N-MOSFET **17**.

Thus, control circuit **470** includes circuitry for intentionally holding N-MOSFET **17** OFF during periods when current reversals would otherwise allow power to be drawn from the load. This feature of the present invention can increase circuit efficiency at low average output current levels when current reversals are most like to occur.

It will be apparent to those of ordinary skill in the art that although comparator **471** monitors the inductor current I_L through feedback current I_{FB2}, other means of detecting current reversals in the inductor current I_L could be used as well. For example, comparator **471** could monitor current feedback signal I_{FB1} just as well so that only one type of

current feedback signal is employed in control circuit **470**. Additionally, many others means of generating a feedback signal indicative of current reversal in inductor current I_L could be used as well (see, e g., resistor R_{SENSE} in FIG. 7).

The high-efficiency control circuit of the present invention was discussed above with respect to FIGS. **1–8** wherein the switching regulator was configured in a voltage step-down configuration. It will be apparent that the control circuit of the present invention could be used in other configurations as well. For example, FIG. **9** shows a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a voltage step-up configuration.

Switching regulator **500** includes synchronously-switched switch **15'** wherein the drains of P-channel MOSFET **16** and N-channel MOSFET **17** are coupled together and to one side of inductor L**1**. The other side of inductor L**1** is coupled to input V_{IN}. Control circuit **70** drives driver circuit **20'** including inverting P-driver **26'** and inverting N-driver **27'**, which in turn drive P-channel MOSFET **16** and N-channel MOSFET **17**, respectively.

Thus, as shown in FIG. **9**, the control circuit of the present invention can be used in switching configurations wherein an input voltage V_{IN} is stepped up to a regulated output voltage V_{OUT}. As is the case with the step-down configurations shown in FIGS. **2–8**, the control circuit of FIG. **9** can be used in other types of step-up configurations as well. For example, one-shot circuit **25** shown in FIG. **9** can include an additional input for monitoring the input voltage V_{IN} to reduce the generation and emission of audible noise from inductor L**1** at low input voltages as discussed above with respect to FIGS. **5** and **6**. Also, switching regulator **500** can include circuitry to hold P-MOSFET **16** OFF during periods when the polarity of inductor current I_L would otherwise reverse, as discussed above with respect to FIG. **8**.

FIG. **10** shows a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a voltage polarity-inversing configuration.

Switching regulator **600** includes switch **15"** wherein the drain of P-channel MOSFET **16** is coupled to one side of inductor L**1** and to V_{OUT} through diode D**601**. The other side of inductor L**1** is coupled to ground. The source of P-channel MOSFET **16** is coupled to the positive input voltage V_{IN}. Control circuit **70'** drives driver circuit **20"** including P-driver **26** which, in turn, drives P-channel MOSFET **16**.

Control circuit **70'** operates substantially similar to control circuit **70** discussed above except for the following. Voltage feedback to control circuit **70'** is provided by resistors R**1** and R**2** and amplifier **602**. Amplifier **602** inverts the negative polarity voltage at V_{OUT} to provide a positive polarity feedback voltage to control circuit **70'**.

Thus, as shown in FIG. **10**, the control circuit of the present invention can be used in switching configurations wherein an input voltage V_{IN} is inverted to a regulated output voltage of opposite polarity V_{OUT}. As is the case with the step-down configurations shown in FIGS. **2–8**, the control circuit of FIG. **10** can be used in other types of polarity-inversing configurations as well. For example, one-shot circuit **25** shown in FIG. **10** can include an additional input for monitoring the input voltage V_{IN} to reduce the generation and emission of audible noise from inductor L**1** at low input voltages. Furthermore, one-shot circuit **25** can include an input for monitoring the output voltage V_{OUT} to control the short circuit current if the output is short circuited as discussed above with respect to FIG. **5** and **6**. Also, if regulator **600** was synchronously switched and included an

N-MOSFET instead of D**601**, the regulator could include circuitry to hold such an N-MOSFET OFF during periods when the polarity of inductor current I_L would otherwise reverse, as discussed above with respect to FIG. **8**.

It will be apparent to those of ordinary skill in the art that although the present invention has been discussed above with reference to a hysteretic voltage comparator for generating the sleep mode control signal to cause the switching regulator to go into and awake from the sleep mode, other means for performing the same function are also possible. For example, if desired, the sleep mode control signal could be generated in response to a monitored output current. Furthermore, the switching regulator could be taken out of the sleep mode a predetermined time period after going into such a mode, instead after the output voltage falls below a predetermined threshold voltage, as illustrated above.

It will also be apparent that although the present invention has been discussed above with reference to FIGS. **1–10**, wherein the power switches were either a pair of complementary MOSFETS (i.e., one p-channel and one n-channel) or a single p-channel MOSFET (FIG. **3**), the present invention is applicable to other types of switches as well. For example, the power switch could include a pair of N-channel MOSFETS, a pair of P-channel MOSFETS, or bipolar junction transistors.

Thus, a control circuit and method for maintaining high efficiency over broad current ranges in a switching regulator circuit has been provided.

One skilled in the art will thus appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.

What is claimed is:

1. A circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the control circuit comprising:

a first circuit for monitoring a signal from the output terminal to generate a first feedback signal;

a second circuit for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the first feedback signal to vary the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage; and

a third circuit for generating a second control signal during a second state of circuit operation to cause both switching transistors to be simultaneously OFF for a period of time if a sensed condition of the regulator indicates that the current supplied to the load falls below a threshold fraction of maximum rated output current for the regulator, whereby operating efficiency of the regulator at low output current levels is improved.

2. The circuit of claim **1** wherein the second control signal is generated in response to the first feedback signal.

3. The circuit of claim **2** wherein the circuit changes from the second to the first state of operation in response to the magnitude of the first feedback signal falling below a first threshold level.

4. The circuit of claim **3** wherein the circuit changes from the first to the second state of operation in response to the magnitude of the first feedback signal exceeding a second threshold level greater than the first threshold level.

5. The circuit of claim 4, wherein the first feedback signal is a voltage feedback signal and the third circuit includes a voltage comparator having hysteresis.

6. The circuit of claim 5, wherein the current consumed by the switching voltage regulator is reduced during the second state of operation.

7. The circuit of claim 1, wherein the second circuit includes:

a one-shot circuit for generating first and second levels of the first control signal during a switch cycle, wherein the first level causes the switch circuit to couple the input voltage to a node of the output circuit, and the second level causes the switch circuit to couple the node of the output circuit to ground.

8. The circuit of claim 7, wherein the second level is generated for a predetermined time period.

9. The circuit of claim 8, wherein the second circuit includes a fourth circuit for monitoring the current supplied to the output terminal to generate a current feedback signal.

10. The circuit of claim 9, wherein the switch is adapted to be coupled to an inductor and the fourth circuit monitors the inductor current to generate the current feedback signal.

11. The circuit of claim 10, wherein the fourth circuit compares the current feedback signal to a reference current value and triggers the one-shot circuit when the current feedback signal exceeds the reference current value.

12. The circuit of claim 11, wherein the fourth circuit includes a current comparator for triggering the one-shot circuit, the current comparator having a first input coupled to receive the current feedback signal and a second input coupled to a current source for providing the reference current value.

13. The circuit of claim 12, wherein the current source includes:

a transconductance amplifier supplying a current substantially proportional to the difference in voltage between the first feedback signal and a constant voltage; and

a constant current source coupled in parallel with the transconductance amplifier.

14. The circuit of claim 7, wherein second level is generated for a time period dependent upon the input voltage.

15. The circuit of claim 14, wherein the switch is coupled to an inductor, and wherein the second level is generated for a time period that is decreased in response to a decrease in the input voltage, whereby the oscillation frequency of the ripple current through said inductor is increased from an audible frequency to one that does not generate substantial user noise.

16. The circuit of claim 7, wherein the second level is generated for a time period that is dependent upon the voltage at the load.

17. The circuit of claim 16, wherein the switch is coupled to an inductor, and wherein the second level is generated for a time period that is increased in response to a decrease in the voltage at the load, whereby the total decrease in current through said inductor during the time period the second level is generated remains substantially constant.

18. The circuit of claim 7, wherein the one-shot circuit is maintained substantially OFF during the second state of operation, whereby the efficiency of the switching regulator circuit is increased as the circuit changes from the first to the second state of operation.

19. The circuit of claim 12, wherein the current comparator is maintained substantially OFF during the second state of operation, whereby the efficiency of the switching regulator circuit is increased as the circuit changes from the first to the second state of operation.

20. The circuit of claim 1, wherein the third circuit includes a user-activated switch and wherein the second control signal is generated in response to activation of the user switch.

21. The circuit of claim 20, wherein:

the second circuit includes a transconductance amplifier supplying a current substantially proportional to the difference in voltage between the feedback signal and a constant voltage during the first state of operation; and

wherein activation of the user switch introduces hysteresis into the transconductance amplifier.

22. The circuit of claim 20, wherein the second circuit includes:

a one-shot circuit for generating first and second levels of the first control signal during a switch cycle, wherein the first level causes the switch circuit to couple the input voltage to a node of the output circuit, and the second level causes the switch circuit to couple the node of the output circuit to ground.

23. The circuit of claim 22, wherein the second level is generated for a predetermined time period.

24. The circuit of claim 23, wherein the second circuit includes a fourth circuit for monitoring the current supplied to the output terminal to generate a current feedback signal.

25. The circuit of claim 24, wherein the fourth circuit compares the current feedback signal to a reference current value and triggers the one-shot circuit when the current feedback signal exceeds the reference current value.

26. The circuit of claim 22, wherein the second level is generated for a time period that is dependent upon the input voltage.

27. The circuit of claim 26, wherein the switch is coupled to an inductor, and wherein the second period of time is decreased in response to a decrease in the input voltage, whereby the oscillation frequency of the ripple current through said inductor is increased from an audible frequency to one that does not generate substantial user noise.

28. The circuit of claim 22, wherein the second level is generated for a time period that is dependent upon the voltage at the load.

29. The circuit of claim 28, wherein the switch is coupled to an inductor, and wherein the second level is generated for a time period that is increased in response to a decrease in the voltage at the load, whereby the total decrease in current through said inductor during the time period the second level is generated remains substantially constant.

30. The circuit of claim 22, wherein the one-shot circuit is maintained substantially OFF during the second state of operation, whereby the efficiency of the switching regulator circuit is increased as the circuit changes from the first to the second state of operation.

31. The circuit of claim 1, wherein the circuit is adapted for controlling a switching voltage regulator circuit having first and second switching transistors coupled in series between an input voltage and ground, wherein the first and second switching transistors are commonly coupled to the output circuit, and wherein the input voltage is higher than the voltage at the load, whereby the switching voltage regulator is a step-down voltage regulator.

32. The circuit of claim 1, wherein the circuit is adapted for controlling a switching voltage regulator circuit wherein the input voltage is lower than the voltage at the load, whereby the switching voltage regulator is a step-up voltage regulator.

33. The circuit of claim 1, wherein the circuit is adapted for controlling a switching voltage regulator circuit wherein the input voltage has an opposite polarity than the voltage at the load, whereby the switching voltage regulator is a polarity-inversing voltage regulator.

34. A circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the control circuit comprising:

a first means for generating a voltage feedback signal indicative of the voltage at the output;

a second means for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the voltage feedback signal to vary the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage; and

a third means for generating a second control signal during a second state of circuit operation to cause both switching transistors to be simultaneously OFF for a period of time if a sensed condition of the regulator indicates that the current supplied to the load falls below a threshold fraction of maximum rated output current for the regulator, the period of time having a duration which is a function of the current supplied to the load by the regulator.

35. The circuit of claim 34, wherein the third means includes a voltage comparator having hysteresis.

36. The circuit of claim 34, wherein the second means includes:

a one-shot circuit for generating first and second levels of the first control signal during a switch cycle, wherein the first level causes the switch circuit to couple the input voltage to a node of the output circuit, and the second level causes the switch circuit to couple the node of the output circuit to ground.

37. The circuit of claim 36, wherein the second means includes a fourth means for monitoring the current supplied to the output terminal to generate a current feedback signal.

38. The circuit of claim 37, wherein the fourth means compares the current feedback signal to a reference current value and triggers the one-shot circuit when the current feedback signal exceeds the reference current value.

39. The circuit of claim 38, wherein the fourth means includes a current comparator for triggering the one-shot circuit, the current comparator having a first input coupled to receive the current feedback signal and a second input coupled to a current source for providing the reference current value.

40. The circuit of claim 39, wherein the current source includes:

a transconductance amplifier supplying a current substantially proportional to the difference in voltage between the feedback signal and a constant voltage; and

a constant current source coupled in parallel with the transconductance amplifier.

41. A method for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the method comprising the steps of:

(a) monitoring a signal from the output terminal to generate a first feedback signal;

(b) varying the duty cycle of the switching transistors in response to the first feedback signal to maintain the output terminal at the regulated voltage during a first state of circuit operation;

(c) turning both switching transistors simultaneously OFF for a period of time during a second state of circuit operation following the first state of circuit operation, so as to allow the output capacitor to maintain the output substantially at the regulated voltage by discharging during the second state of circuit operation, the period of time beginning when the current supplied to the load falls below a threshold fraction of maximum rated output current for the regulator, and having a duration which is a function of the current supplied to the load by the regulator; and

(d) turning at least one of said switching transistors ON to recharge the output capacitor following the second state of circuit operation.

42. The method of claim 41, wherein the switching voltage regulator includes a one-shot circuit for varying the duty cycle of the switching transistors and wherein step (c) includes the step of maintaining the one-shot circuit substantially OFF during the second state of operation.

43. The method of claim 2, wherein the switching voltage regulator includes a current comparator for triggering the one-shot circuit and wherein step (c) includes the step of maintaining the current comparator substantially OFF during the second state of operation.

44. A circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output inductor coupled thereto for supplying current at a regulated voltage to a load, the circuit comprising:

a first circuit for monitoring a signal from the output terminal to generate a first feedback signal;

a second circuit for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the first feedback signal to vary the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage; and

a third circuit for monitoring the current to the output terminal to generate a second control signal during a second state of circuit operation when the monitored current compares in a predetermined manner to a threshold indicative of a polarity reversal condition in the output inductor, said second state causing one of said switching transistors to be maintained OFF, such that the switch circuit is prevented from coupling the output circuit to ground.

45. The circuit of claim 44 wherein the third circuit monitors the current through the inductor to generate the second control signal when the magnitude of the inductor current falls below the current threshold.

46. The circuit of claim 44 wherein the third circuit prevents reversals in polarity of the current through the inductor.

47. The circuit of claim 46, wherein the first feedback signal is a voltage feedback signal and the third circuit includes a current comparator for comparing the monitored current to the current threshold.

48. The circuit of claim 47, wherein the current consumed by the switching voltage regulator is reduced during the second state of operation.

49. The circuit of claim 44, wherein the second circuit includes:

a one-shot circuit for generating first and second levels of the first control signal during a switch cycle, wherein the first level causes the switch circuit to couple the input voltage to a node of the output circuit, and the second level causes the switch circuit to couple the node of the output circuit to ground.

50. The circuit of claim **49**, wherein the second level is generated for a predetermined time period.

51. A method for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output inductor coupled thereto for supplying current at a regulated voltage to a load, the method comprising the steps of:

(a) monitoring a signal from the output terminal to generate a first feedback signal;

(b) varying the duty cycle of the switching transistors in response to the first feedback signal to maintain the output terminal at the regulated voltage during a first state of circuit operation, wherein the current to the load has a polarity; and

(c) maintaining one of said switching transistors OFF for a period of time following the first state of circuit operation to de-couple the output circuit from ground during the period of time so as to prevent the current to the load from reversing polarity.

52. The method of claim **51** wherein step (c) includes step (d) of monitoring the current to the output terminal and detecting when the current falls below a current threshold.

53. The method of claim **52** wherein step (d) includes monitoring the current through the inductor.

54. The circuit of claim **53**, wherein the current consumed by the switching voltage regulator is reduced during the second state of operation.

55. A circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the control circuit comprising:

drive circuitry for the pair of synchronously switched switching transistor;

feedback circuitry, coupled to the drive circuitry to control the duty cycle of the pair of synchronously switched switching transistors, the feedback circuitry forming a feedback path in the regulator between the output circuit and the drive circuitry by which feedback information indicative of the current supplied to the load by the regulator conditions the duty cycle of the pair of synchronously switched switching transistors; and

logic circuitry, coupled to the feedback circuitry and the drive circuitry, which prevents the drive circuitry from turning on either of the pair of synchronously switched switching transistors if the feedback information indicates that the current supplied to the load by the regulator falls below selected sleep mode current level, wherein the synchronously switched switching transistors are prevented from being turned on for a period of time that is a function of the current supplied to the load by the regulator.

56. The circuit of claim **55** wherein:

the output circuit includes an inductor coupled to the pair of synchronously switched switching transistors and the output terminal;

the feedback information includes a first feedback signal derived by sensing current conducted between the inductor and the output terminal and a second feedback signal derived by sensing voltage at the output terminal; and

the feedback circuitry includes a comparator circuit that compares the first feedback signal to an error signal generated from the second feedback signal to control switching between the pair of synchronously switched switching transistors, and a threshold circuit that sets a minimum inductor current value at which the drive circuitry switches between transistors.

57. An improved circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, and wherein the control circuit varies the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage, the improvement comprising:

circuitry incorporated in the control circuit for detecting a condition in the output circuit indicative of the current supplied to the load falling below a threshold fraction of maximum rated output current for the regulator and for turning off both switching transistors simultaneously for a period of time if the supplied current falls below the threshold, the period of time having a duration which is a function of the current supplied to the load by the regulator.

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EXHIBIT B

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Wilcox et al.

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(54) **CONTROL CIRCUIT AND METHOD FOR MAINTAINING HIGH EFFICIENCY OVER BROAD CURRENT RANGES IN A SWITCHING REGULATOR CIRCUIT**

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(51) **Int. Cl.**[7] **G05F 1/40**
(52) **U.S. Cl.** **323/282**; 323/272
(58) **Field of Search** 323/282, 280, 323/281, 283, 284, 286, 272, 266

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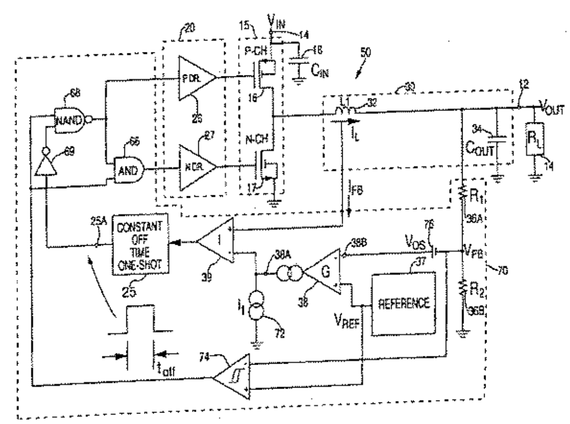
(57) **ABSTRACT**

A circuit and method for controlling a switching voltage regulator having (1) a switch including one or more switching transistors and (2) an output adapted to supply current at a regulated voltage to a load including an output capacitor. The circuit and method generates a control signal to turn said one or more switching transistors OFF under operating conditions when the voltage at the output is capable of being maintained substantially at the regulated voltage by the charge on the output capacitor. Such a circuit and method increases the efficiency of the regulator circuit particularly at low average current levels.

35 Claims, 10 Drawing Sheets



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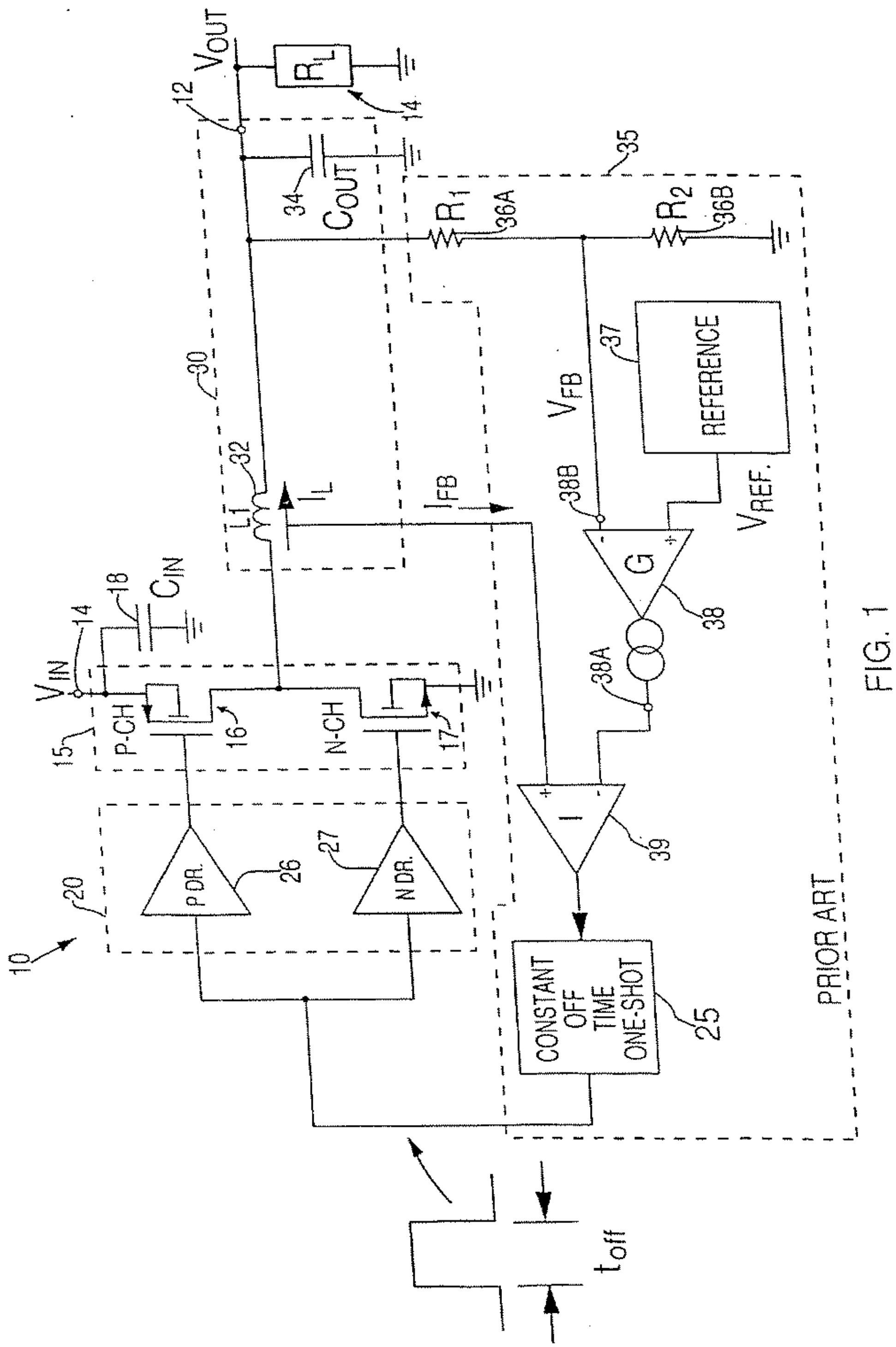
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V_FB
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C_IN
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P-CH
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PRIOR ART
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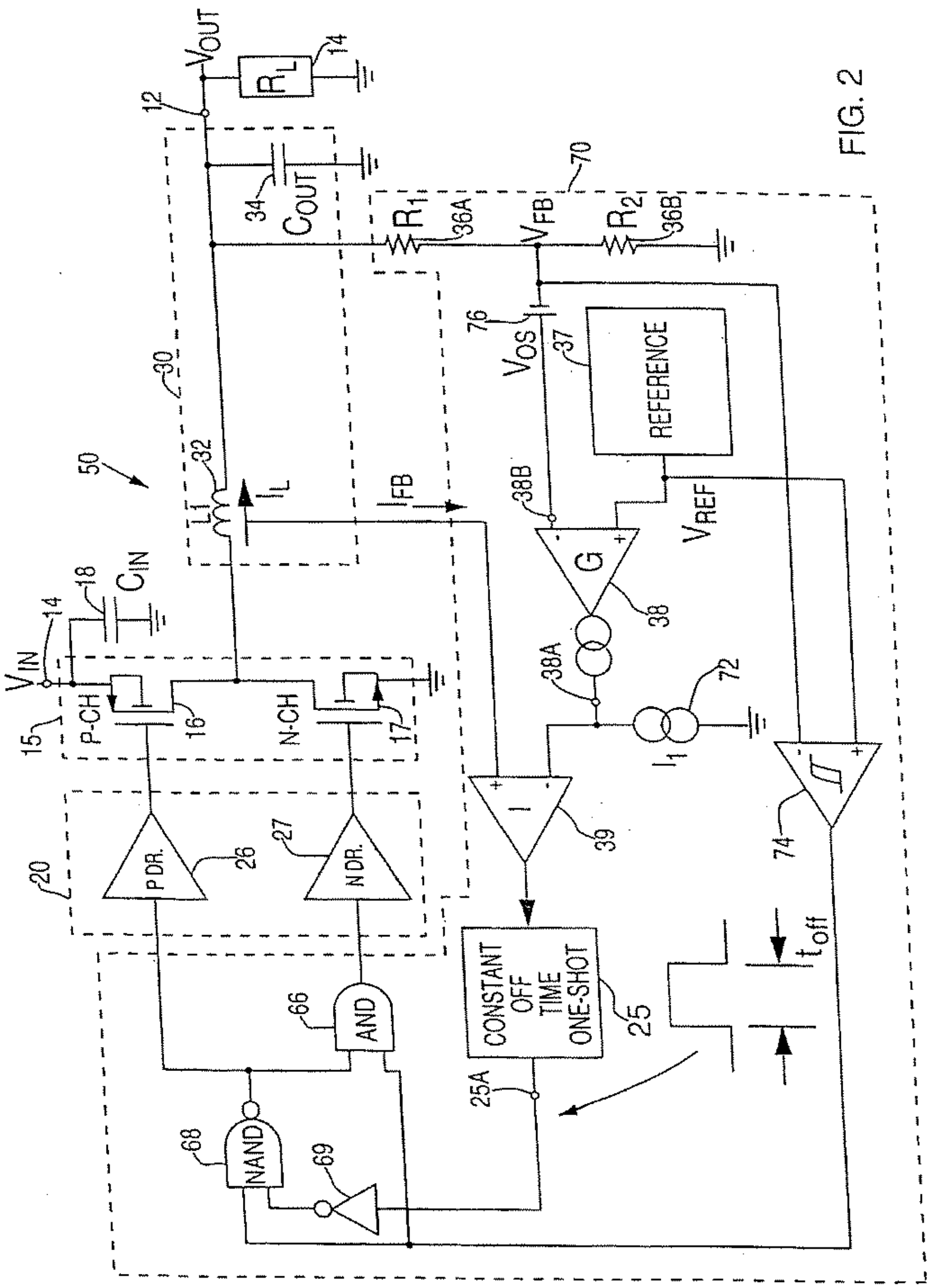
FIG. 1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76
VOS
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REFERENCE
38B
G
38
VREF
VIN
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CIN
15
P-CH
16
N-CH
17
38A
72
I1
39
74
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AND
CONSTANT OFF TIME ONE-SHOT
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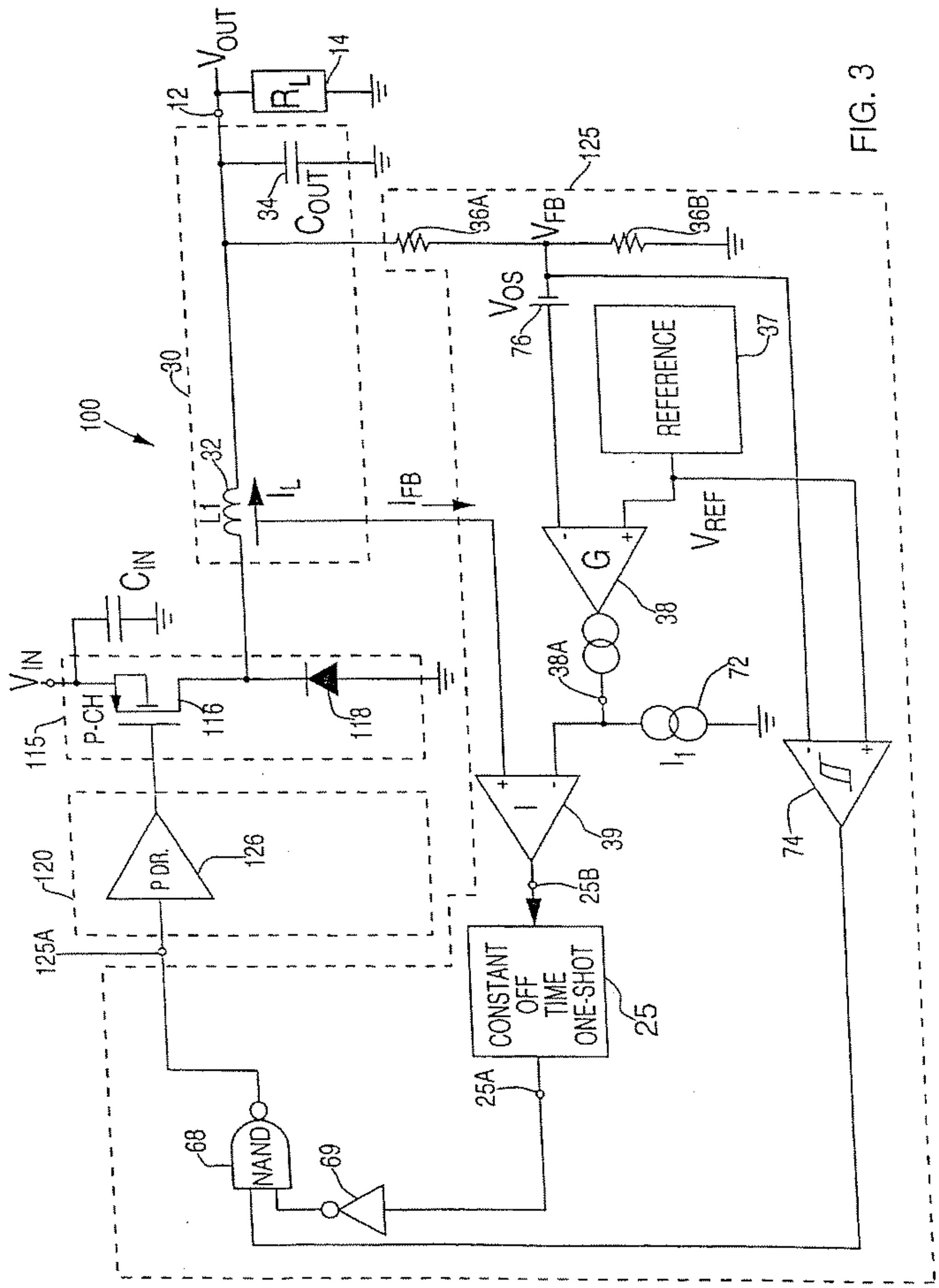
25A
toff
68
NAND
69

FIG. 2



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REFERENCE
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38A
72
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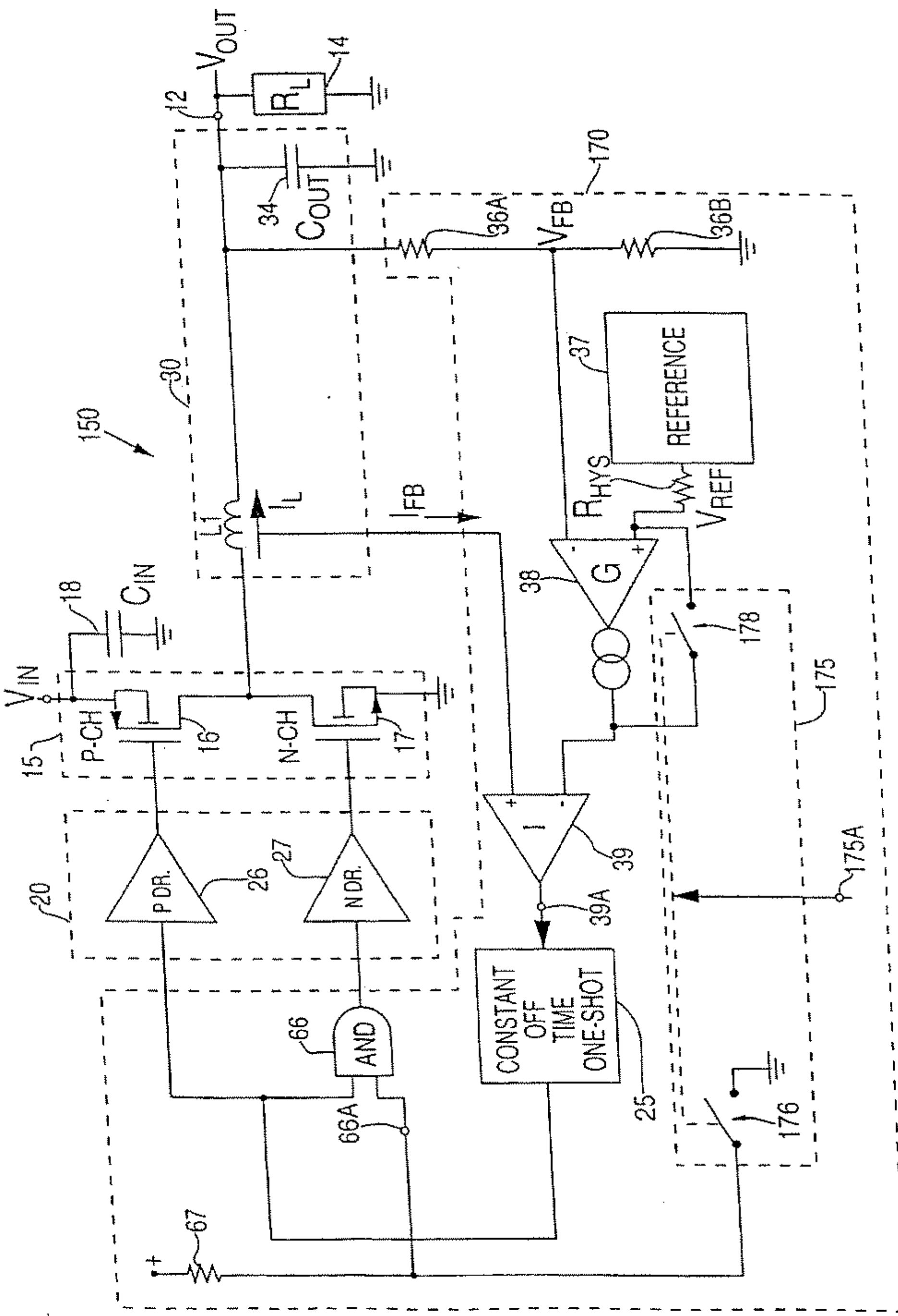
FIG. 3



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N-CH
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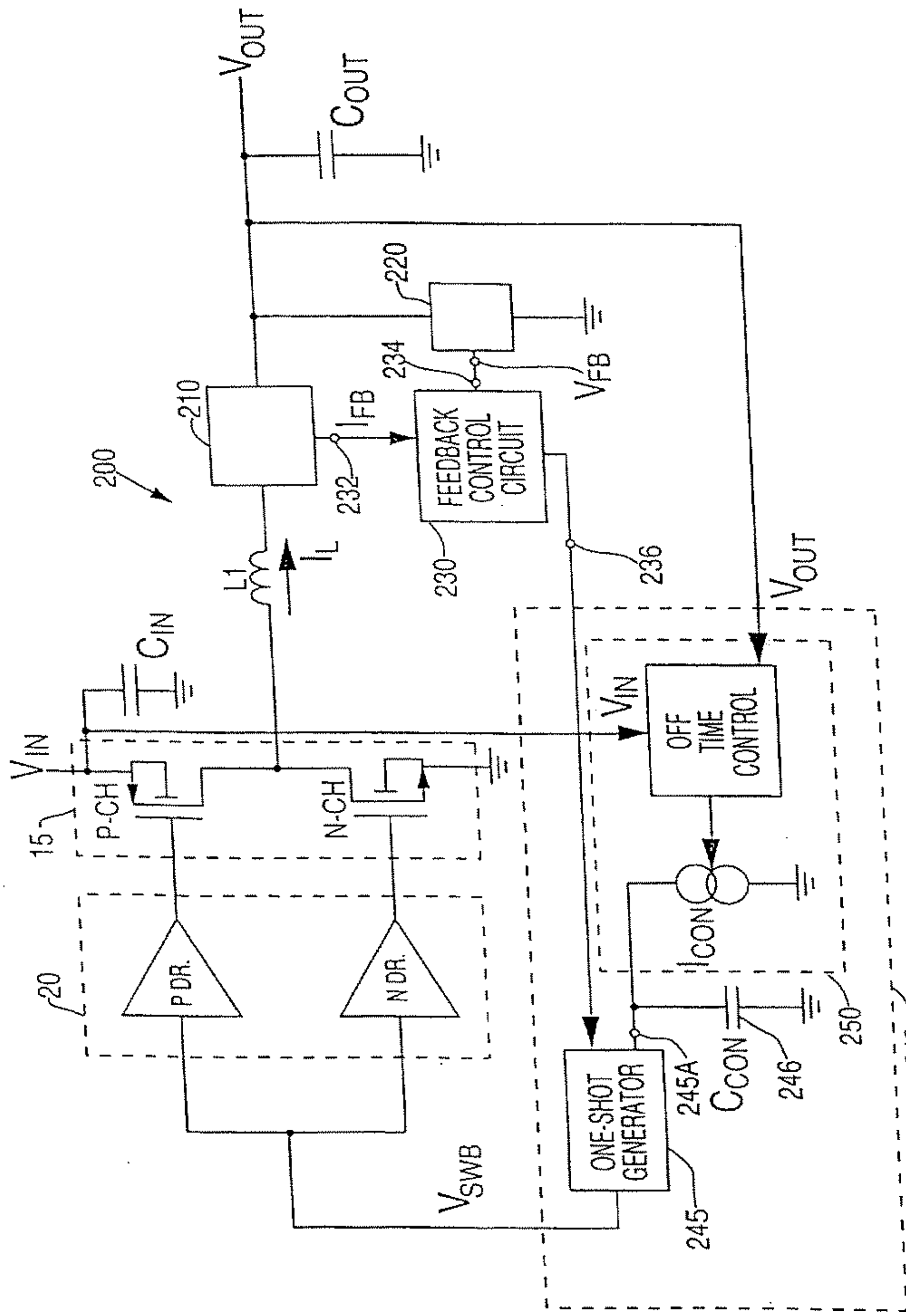
N DR.
AND
CONSTANT OFF TIME ONE-SHOT
G
I

FIG. 4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OFF TIME CONTROL
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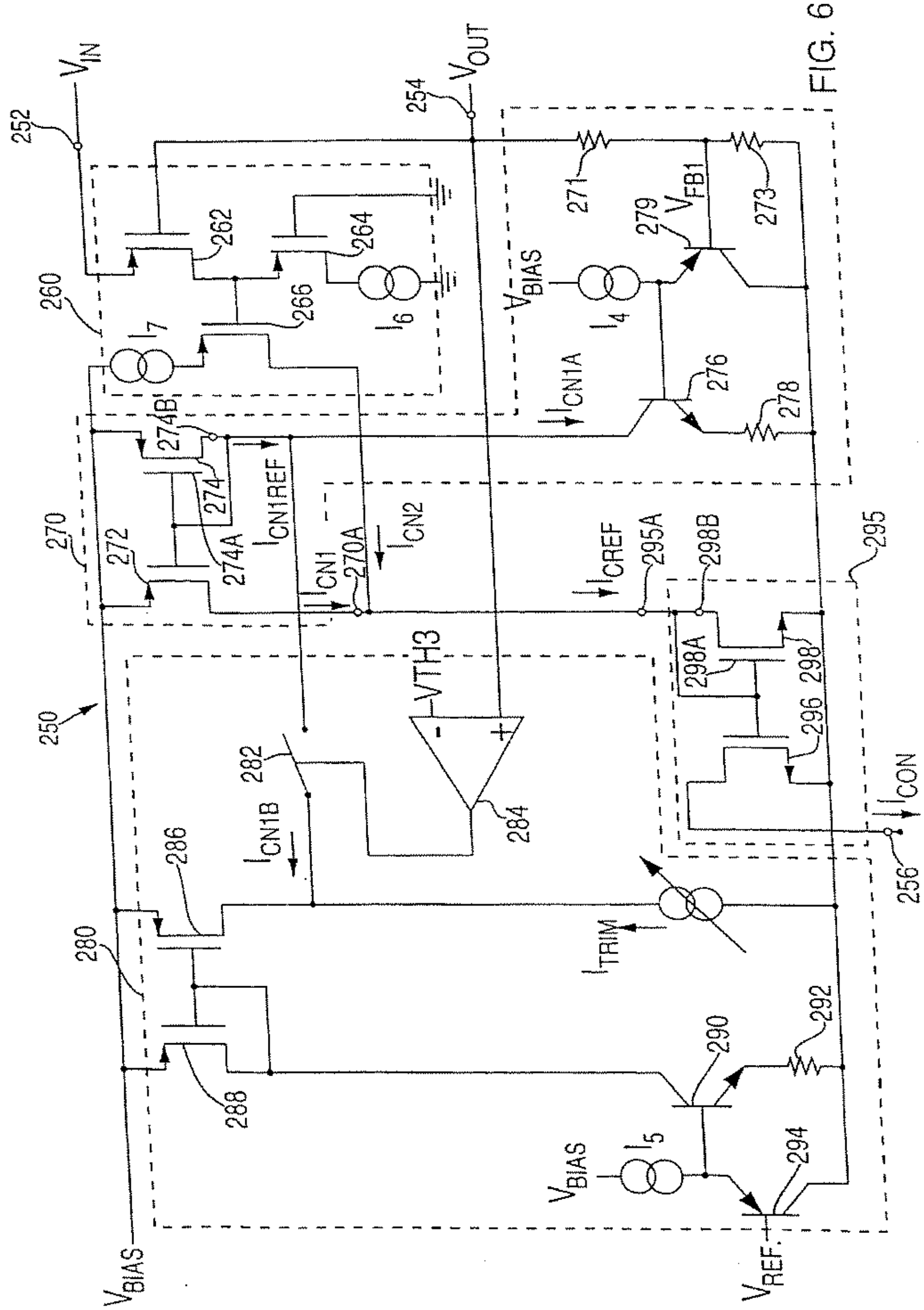
V_{SWB}

FIG. 5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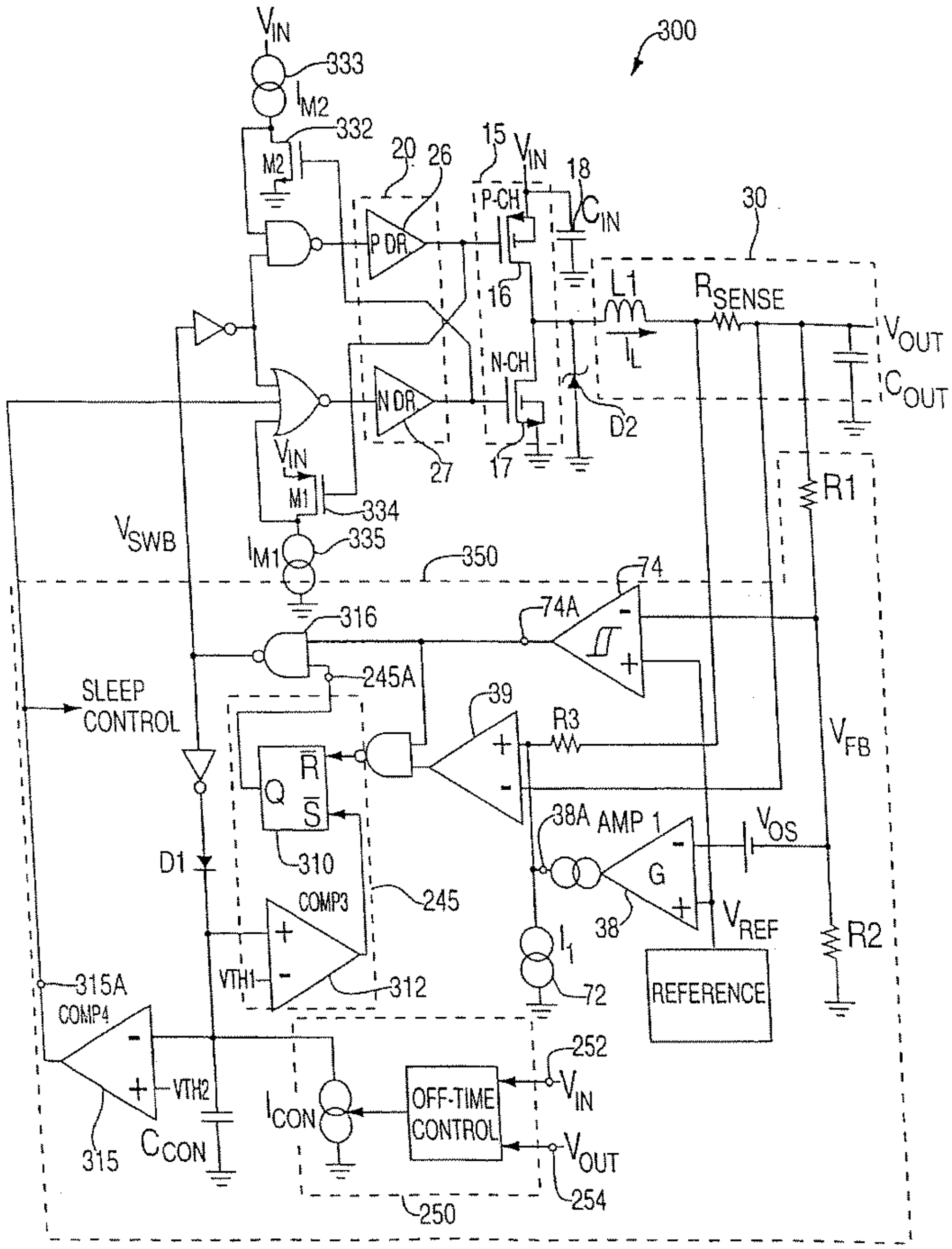
298
296
I_{CON}
256
250
VTH3
282
284
I_{CN1B}
286
280
288
I_{TRIM}
290
292
V_{BIAS}
I_5
294
$V_{REF.}$
V_{BIAS}

FIG. 6



300
V_{IN}
333
I_{M2}
332
M2
20
26
15
V_{IN}
18
P-CH
C_{IN}
30
P DR
16
L1
R_{SENSE}
V_{OUT}
I_L
N-CH
N DR
C_{OUT}
D2
V_{IN}
27
17
M1
334
R1
V_{SWB}
I_{M1}
335
350
74
316
74A
245A
SLEEP CONTROL
39
R3
V_{FB}
Q
R
S
38A AMP 1
V_{OS}
G
D1
310
COMP3
245
38
V_{REF}
I_1
R2
VTH1
312
315A
72
COMP4
REFERENCE
252
V_{IN}
VTH2
OFF-TIME CONTROL
I_{CON}
V_{OUT}
315
C_{CON}
254
250

FIG. 7

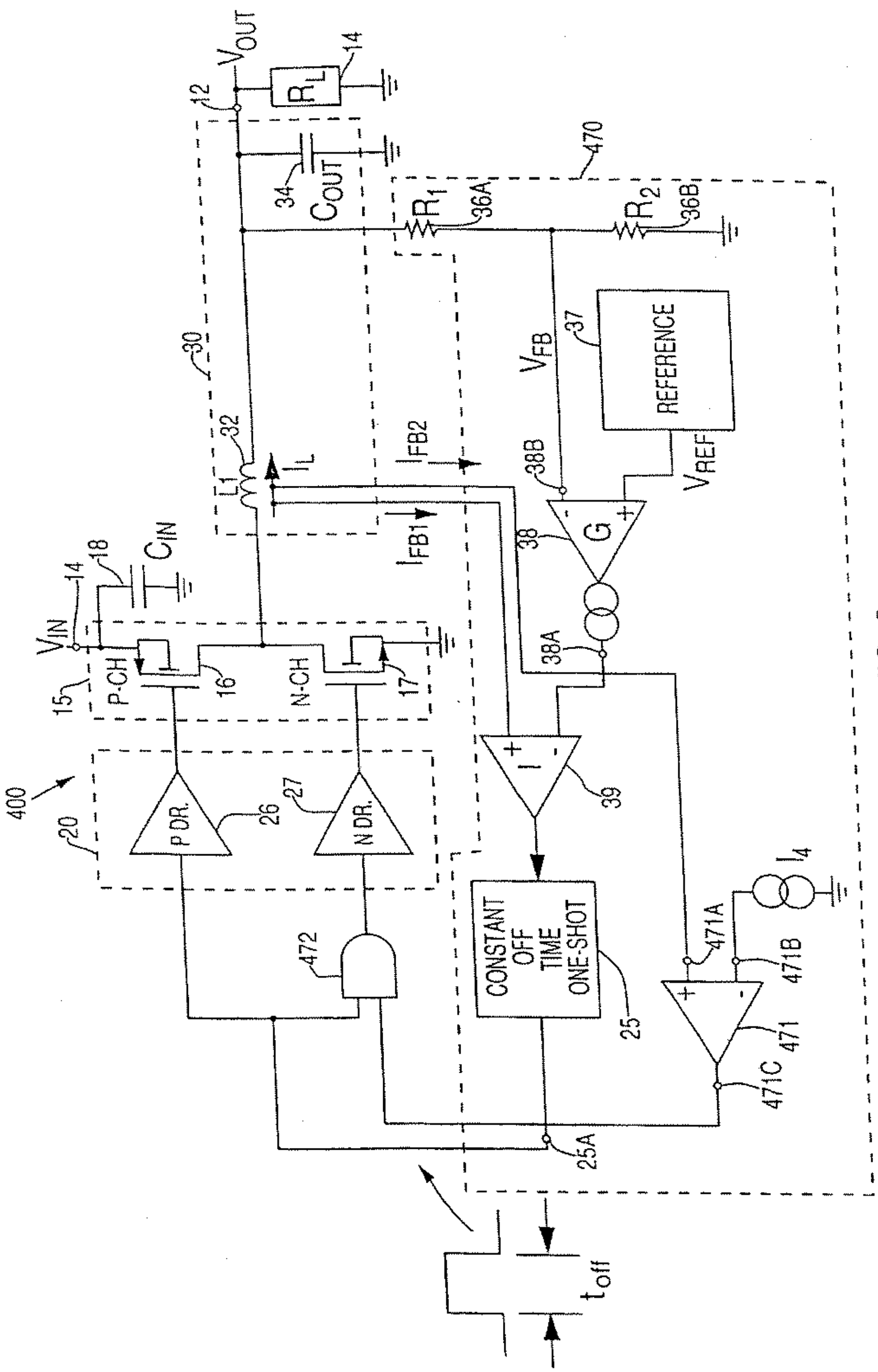
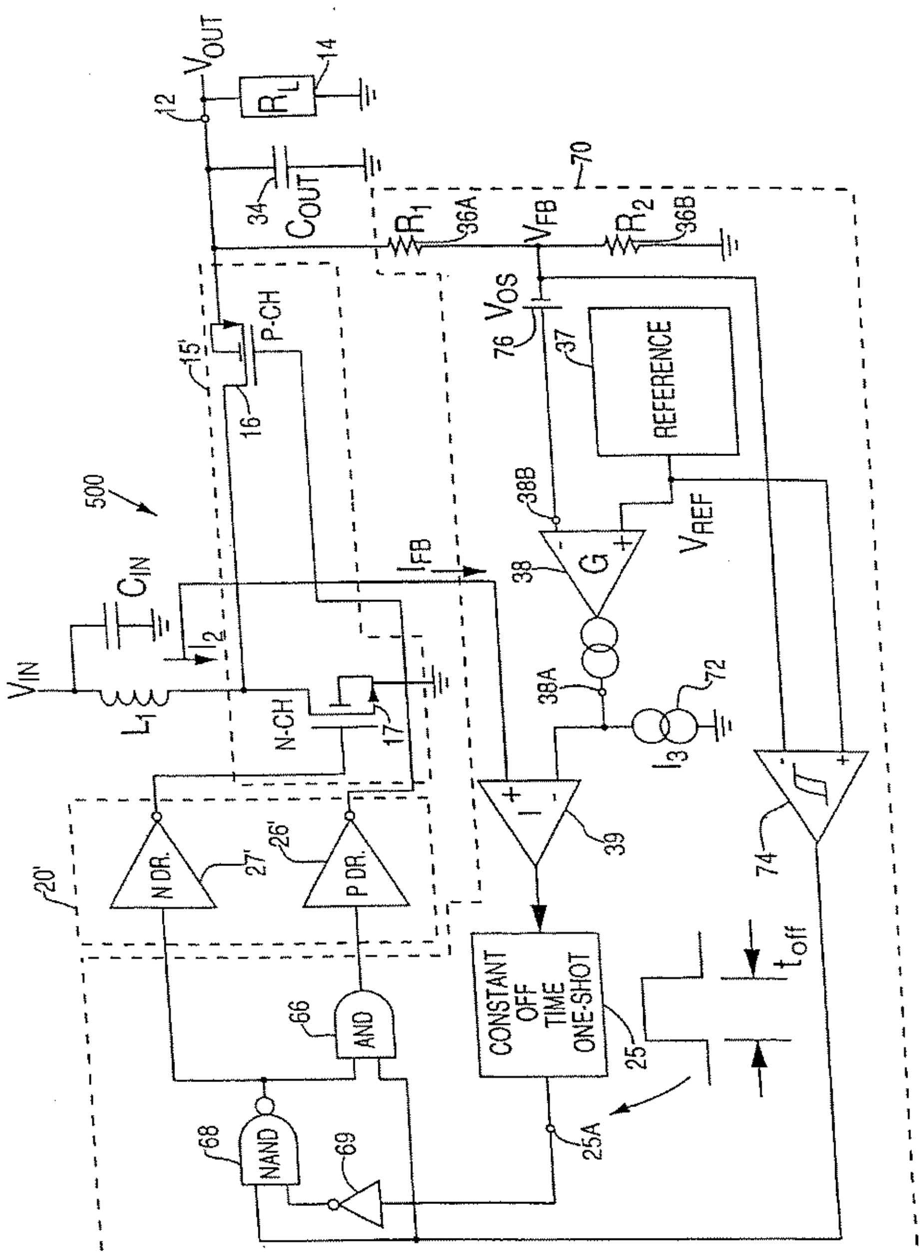

VOUT
RL
CIN
VIN
P-CH
N-CH
P DR.
N DR.
REFERENCE
VFB
VREF
IL
IFB1
IFB2
L1
COUT
R1
R2
G
I
I4
CONSTANT OFF TIME ONE-SHOT
toff
400
470
472
471
471A
471B
471C
25A

FIG. 8



500
V_{IN}
L_1
C_{IN}
I_2
N-CH
17
16
15'
P-CH
12
V_{OUT}
R_L
14
34
C_{OUT}
R_1
36A
V_{FB}
R_2
36B
70
76
V_{OS}
37
REFERENCE
38B
38
G
V_{REF}
I_{FB}
38A
72
I_3
39
74
20'
N DR.
27'
P DR.
26'
66
AND
68
NAND
69
CONSTANT OFF TIME ONE-SHOT
25
25A
t_{off}

FIG. 9

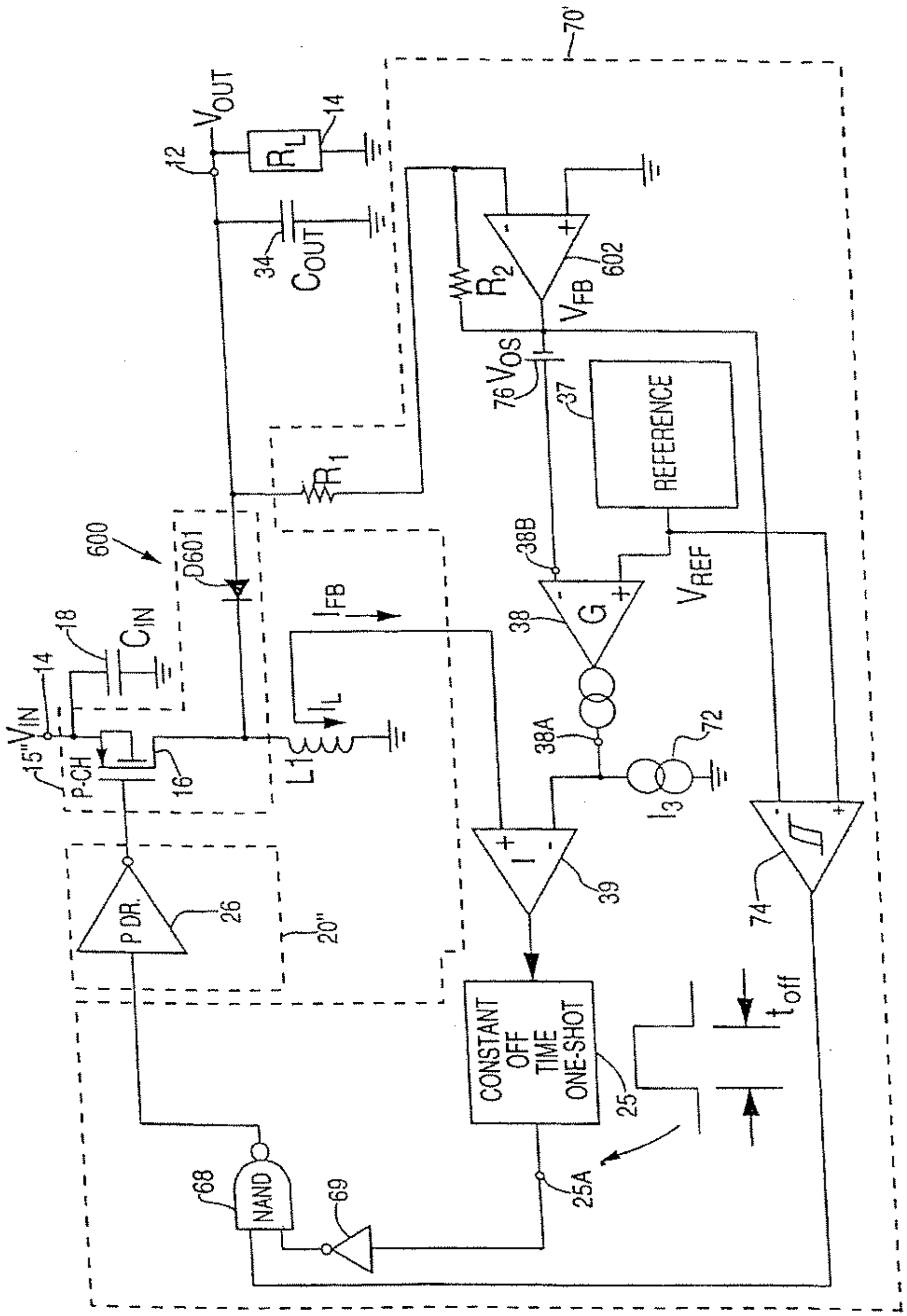

70'
12
V_{OUT}
14
R_L
34
C_{OUT}
R_2
602
V_{FB}
76
V_{OS}
37
REFERENCE
R_1
600
D601
18
C_{IN}
14
V_{IN}
15''
P-CH
16
L1
I_L
I_{FB}
38B
38
G
V_{REF}
38A
72
I_3
39
I
74
P DR.
26
20''
CONSTANT OFF TIME ONE-SHOT
25
t_{off}
25A
68
NAND
69

FIG. 10

CONTROL CIRCUIT AND METHOD FOR MAINTAINING HIGH EFFICIENCY OVER BROAD CURRENT RANGES IN A SWITCHING REGULATOR CIRCUIT

The present application is a continuation of application Ser. No. 09/395,895, filed Sep. 14, 1999, now U.S. Pat. No. 6,304,066, which is a continuation of application Ser. No. 08/978,167, filed Nov. 26, 1997, now U.S. Pat. No. 5,994, 885, which is a division of application Ser. No. 08/799,467, filed Feb. 13, 1997, now U.S. Pat. No. 5,731,694, which is a continuation of application Ser. No. 08/634,688, filed Apr. 18, 1996 now abandoned, which is a continuation of application Ser. No. 08/476,232, filed Jun. 07, 1995 now abandoned, which is a division of application Ser. No. 08/036,047, filed Mar. 23, 1993, now U.S. Pat. No. 5,481, 178.

BACKGROUND OF THE INVENTION

The present invention relates to a switching regulator circuit. More particularly, the present invention relates to a control circuit and method for maintaining high efficiency over broad current ranges in a switching regulator circuit.

The purpose of a voltage regulator is to provide a predetermined and constant output voltage to a load from a poorly-specified and fluctuating input voltage source. Generally, there are two different types of regulators: series regulators and switching regulators.

The series regulator employs a pass element (e.g., a power transistor) coupled in series with a load and controls the voltage drop across the pass element in order to regulate the voltage which appears at the load. In contrast, the switching regulator employs a switch (e.g., a power transistor) coupled either in series or parallel with the load. The regulator controls the turning ON and turning OFF of the switch in order to regulate the flow of power to the load. The switching regulator employs inductive energy storage elements to convert the switched current pulses into a steady load current. Thus, power in a switching regulator is transmitted across the switch in discrete current pulses, whereas in a series regulator, power is transmitted across the pass element as a steady current flow.

In order to generate a stream of current pulses, switching regulators typically include control circuitry to turn the switch on and off. The switch duty cycle, which controls the flow of power to the load, can be varied by a variety of methods. For example, the duty cycle can be varied by either (1) fixing the pulse stream frequency and varying the ON or OFF time of each pulse, or (2) fixing the ON or OFF time of each pulse and varying the pulse stream frequency.

Which ever method is used to control the duty cycle, switching regulators are generally more efficient than series regulators. In series regulators, the pass element is generally operated in its linear region where the pass element conducts current continuously. This results in the continuous dissipation of power in the pass transistor. In contrast, in switching regulators, the switch is either OFF, where no power is dissipated by the switch, or ON in a low impedance state, where a small amount of power is dissipated by the switch. This difference in operation generally results in reduced amounts of average power dissipation in switching regulators.

The above difference in efficiency can be more apparent when there is a high input-output voltage difference across the regulator. For example, it would not be unusual for a series regulator to have an efficiency of less than 25 percent

when a switching regulator could perform an equivalent function with an efficiency of greater than 75 percent.

Because of their improved efficiency over series regulators, switching regulators are typically employed in battery-operated systems such as portable and laptop computers and hand-held instruments. In such systems, when the switching regulator is supplying close to the rated output current (e.g., when a disk or hard drive is ON in a portable or laptop computer), the efficiency of the overall circuit can be high. However, the efficiency is generally a function of output current and typically decreases at low output current. This reduction in efficiency is generally attributable to the losses associated with operating the switching regulator. These losses include, among others, quiescent current losses in the control circuitry of the regulator, switch losses, switch driver current losses and inductor/transformer winding and core losses.

The reduction in efficiency of a switching regulator at low output current can become important in battery-operated systems where maximizing battery lifetime is desirable.

In view of the foregoing, it would be desirable to provide a high efficiency switching regulator.

It would also be desireable to provide a control circuit and method for maintaining high efficiency over broad current ranges, including low output currents, in a switching regulator circuit.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a high efficiency switching regulator.

It is also an object of the present invention to provide a control circuit and method for maintaining high efficiency over broad current ranges, including low output currents, in a switching regulator circuit.

In accordance with these and other objects of the invention, there is provided a circuit and method for controlling a switching voltage regulator having (1) a switch including one or more switching transistors and (2) an output adapted to supply current at a regulated voltage to a load including an output capacitor. The circuit and method generates a control signal to turn the one or more switching transistors OFF under operating conditions when the voltage at the output is capable of being maintained substantially at the regulated voltage by the charge on the output capacitor (e.g., during low output currents). During such periods of time, the load does not consume power from the input power source. Therefore, the regulator efficiency is increased. If desired, other components in the switching regulator, in addition switching transistors, can also be intentionally held OFF to conserve additional power. This additional feature of the present invention can further increase the efficiency of the overall regulator circuit.

The circuit and method of the present invention can be used to control various types of switches in switching regulator circuits, including switches that use either one or more power transistors. Additionally, the circuit and method can be used to control switches in various types of switching regulator configurations, including voltage step-down, voltage step-up and polarity-inversing configurations.

Additionally, the circuit and method of the present invention can vary the OFF time of the switching transistor in response to the input and output voltages of the switching regulator. This feature of the present invention reduces the emission of audible noise from the switching regulator during low input voltage conditions. It also reduces the

potential for current runaway during short circuits in the output voltage for some regulator configurations.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the present invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. 1 is a schematic block diagram of a typical prior art switching regulator circuit employing a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 2 is a schematic block diagram of a switching regulator circuit incorporating a first embodiment of the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 3 is a schematic block diagram of a switching regulator circuit incorporating a second embodiment of the high-efficiency control circuit of the present invention to drive a switch including a switching MOSFET and a switching diode in a step-down configuration;

FIG. 4 is a schematic block diagram of a switching regulator circuit incorporating a "user-activated" embodiment of the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 5 is a schematic block diagram of a switching regulator circuit incorporating the variable OFF-time control circuit of the present invention;

FIG. 6 is a detailed schematic diagram of an embodiment of the variable OFF-time control circuit of FIG. 5;

FIG. 7 is a detailed schematic block diagram of an exemplary switching regulator circuit incorporating both the variable OFF-time feature and the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration;

FIG. 8 is a schematic block diagram of a switching regulator circuit incorporating a circuit of the present invention for preventing reversals in the polarity of the current in the output inductor of the regulator from drawing power from the load;

FIG. 9 is a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a step-up configuration; and

FIG. 10 is a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a polarity-reversing configuration.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic block diagram of a typical prior art switching regulator circuit employing a push-pull switch in a step-down configuration.

Referring to FIG. 1, circuit **10** is used to provide a regulated DC output voltage V_{OUT} at terminal **12** (e.g., 5 volts) for driving load **14** which, for example, may be a portable or laptop computer or other battery-operated system. Circuit **10** operates from an unregulated supply voltage V_{IN} coupled to terminal **14** (e.g., a 12 volt battery). Circuit **10** includes push-pull switch **15**, driver circuit **20**, output circuit **30** and control circuit **35**.

Driver circuit **20** is used to drive push-pull switch **15** which includes two synchronously-switched power MOSFETS **16** (p-channel) and **17** (n-channel) stacked in series between supply rail V_{IN} and ground. Push-pull switch **15** in conjunction with driver circuit **20** is typically referred to as a "half-bridge" configuration. MOSFETS **16** and **17** are used to alternately supply current to output circuit **30** which includes inductor **32** (L1) and output capacitor **34** (C_{OUT}). Output circuit **30** smooths the alternating supply of current so that load **12** is provided a regulated voltage V_{OUT}. In order to supply the alternating current, MOSFETS **16** and **17** are respectively driven by P-channel driver **26** and N-channel driver **27**, which in turn are both controlled by control circuit **35**.

Control circuit **35** includes one-shot circuit **25** which provides an OFF pulse of constant duration (e.g., 2 to 10 microseconds) during which time MOSFET **16** is held OFF and MOSFET **17** is held ON by drivers **26** and **27**, respectively. Otherwise, one-shot circuit **25** provides an ON pulse during which time MOSFET **16** is held ON and MOSFET **17** is held OFF. Therefore, one-shot circuit **25** alternately turns MOSFETS **16** and **17** ON and OFF to provide an alternating supply of current to (output circuit **30**. The duty cycle of the one-shot circuit **35** is in turn controlled by current amplifier **39**.

Control circuit **35** monitors the output voltage V_{OUT} through resistor-divider network R_1/R_2 (**36A/36B**) to provide a feedback voltage V_{FB} proportional to the output voltage V_{OUT}. Control circuit **35** also monitors the current I_L through inductor L1 to provide a feedback current I_{FB} proportional to inductor current I_L. Circuit **10** operates by controlling inductor current I_L so that the feedback voltage V_{FB} is regulated to be substantially equal to a reference voltage V_{REF} provided by reference circuit **37**. With feedback voltage V_{FB} being regulated, the output voltage V_{OUT} is in turn regulated to a higher voltage by the ratio of (R_1+to R_2) to R_2.

Transconductance amplifier **38** is used to compare the feedback voltage V_{FB} to a reference voltage V_{REF}. Circuit **10** regulates the output voltage V_{OUT} as follows. During each cycle when switch **15** is "ON", P-MOSFET **16** is turned ON and the current I_L in inductor L1 ramps up at a rate dependent on V_{IN}–V_{OUT}. When I_L ramps up to a threshold level set by output **38A** of transconductance amplifier **38**, current comparator **39** trips and triggers the one-shot OFF pulse, initiating the "OFF" cycle of switch **15**. During the "OFF" cycle, one-shot circuit **25** holds P-MOSFET **16** OFF and turns N-MOSFET **17** ON. This in turn causes the current I_L in inductor L1 to ramp down at a rate dependent on V_{OUT}. Thus, the duty cycle of the periodic turning OFF of switch **15** is controlled so the current I_L produces a regulated output voltage V_{OUT} at terminal **12**.

As the output load current increases, the voltage drop across R_2 resistor **36B** will decrease. This translates into a small error voltage at input **38B** of transconductance amplifier **38** that will cause output **38A** to increase, thus setting a higher threshold for current comparator **39**. Consequently, current I_L in inductor L1 is increased to the level required to support the load current.

Since the OFF time (t_{OFF}) of one-shot circuit **25** is constant, switching regulator circuit **10** has a constant ripple current in inductor L1 (for constant output voltage V_{OUT}), but has a frequency which varies with V_{IN}. The ripple oscillation frequency is given by the equation:

$$f_{RIP}=(1/t_{OFF})[1-(V_{OUT}/V_{IN})]$$

One disadvantage of circuit **10** in FIG. **1** is that the ripple oscillation frequency f_{RIP} may decrease to an audible level with low input voltages V_{IN}. This could occur, for example, when a battery powering the switching regulator circuit is nearly discharged. Inductor L1 may then generate and emit noise that can be objectionable to a user of the device employing the regulator circuit.

An additional disadvantage of prior art circuit **10** is that the inductor current I_L is not well controlled when the output voltage V_{OUT} is shorted to ground. The basic relationship between inductor current and voltage is given by the equation di/dt=V/L. This means that the rate at which current I_L in inductor L1 decays during the OFF-time depends on the voltage across inductor L1, which is the sum of V_{OUT} and the drain to source voltage, V_{DS}, of N-MOSFET **17**. During a short, V_{OUT} approaches zero while V_{DS} is also very low, resulting in very little decay of current I_L in inductor L1 during t_{OFF} However, following each OFF cycle, P-MOSFET **16** is turned back ON until current comparator **39** again trips one-shot constant OFF time control circuit **25**. Even for the minimum time that P-MOSFET **16** is ON, the current I_L in inductor L1 may increase by more than it can decrease during t_{OFF} This may result in a runaway condition in which the short circuit current may reach destructive levels.

A further disadvantage of prior art circuit **10** results from the constant ripple current in inductor L1. During t_{OFF} current I_L in inductor L1 always ramps down by the same amount regardless of the output current of the regulator. At low output currents this can cause the current in inductor L1 to reverse polarity and, thus, pull power from the load. During the following ON cycle, this current again ramps positive such that the average inductor current equals the load current. Losses associated with this constant ripple current, along with switching losses due to the charging and discharging of switch **15**'s MOSFET gates, can produce large reductions in efficiency at low output currents. This will be especially the case if the current in inductor L1 reverses and power is pulled from the load to ground through N-MOSFET **17**.

A still further disadvantage of prior art circuit **10** concerns the gate drives to P-MOSFET **16** and N-MOSFET **17**. Delays are generally incorporated into drivers **26** and **27** to ensure that one power MOSFET turns OFF before the other turns ON. If there is insufficient deadtime between the conduction of the two MOSFETs (due to, for example, device, circuit processing, or temperature variations), current will be passed directly from input supply V_{IN} to ground. This "shoot-through" effect can dramatically reduce efficiency, and in some circumstances, can overheat and destroy the power MOSFETs.

FIG. **2** is a schematic block diagram of a switching regulator circuit incorporating a first embodiment of the high-efficiency control circuit of the present invention for driving a switch including a pair of synchronously-switched MOSFETS in a step-down configuration.

Switching regulator circuit **50** includes push-pull switch **15**, driver circuit **20** and output circuit **30** similar to those of FIG. **1**. Circuit **50** also includes an embodiment **70** of the high-efficiency control circuit of the present invention.

Control circuit **70** includes one-shot circuit **25**, current comparator **39** and amplifier **38** similar to those of FIG. **1**. However, in addition to those components, control circuit **70** also includes constant current source I_1 **72** and hysteretic comparator **74** for providing high efficiency operation at low average current levels.

As will be discussed in greater detail below, constant current source I_1 **72** and comparator **74** allow push-pull switch **15** to go into a state of operation where both MOSFETS **16** and **17** are simultaneously OFF under conditions where the output voltage V_{OUT} can be maintained substantially at the regulated voltage V_{REG} by output capacitor C_{OUT}. This state of operation is referred to herein as a "sleep mode." The ability of push-pull switch **15** to go into such a sleep mode is in contrast to the regulator circuit of FIG. **1** where one of the two MOSFETs **16** and **17** is substantially ON at all times. This feature of the present invention reduces the regulator circuit power consumption since push-pull switch **15** does not dissipate power or allow power to be pulled from load R_L to ground in sleep mode.

Furthermore, if desired, while push-pull switch **15** is in the above-described sleep mode, the regulator circuit can turn OFF other circuit components which are not needed while the regulator is in sleep mode. For example, for the embodiment of the present invention shown in FIG. **2**, one-shot circuit **25**, current comparator **39**, current source I_1 **72** and amplifier **38** can also be turned OFF in sleep mode. This feature of the present invention allows the regulator circuit to operate at even higher efficiencies than otherwise possible if only push-pull switch **15** were maintained in a sleep mode.

At high load current levels (e.g., greater than 20 percent of the maximum rated output current) control circuit **70** operates similar to control circuit **35** of FIG. **1**. In FIG. **2**, the current feedback I_{FB} is again provided to the non-inverting input of current comparator **39**. Offset V_{OS} **76**, which preferably is built into amplifier **38**, level-shifts feedback voltage V_{FB} slightly below reference voltage V_{REF}, thus keeping the output of hysteretic comparator **74** high during high current conditions. When the feedback current I_{FB} exceeds the current supplied to the inverting input of current comparator **39**, the output of comparator **39** goes HIGH so as to initiate the switch "OFF" cycle.

During the "OFF" cycle, output **25A** of one-shot circuit **25** is HIGH, which turns P-MOSFET **16** OFF and N-MOSFET **17** ON. After a constant time set by one-shot circuit **25**, output **25A** goes LOW, thus initiating the next "ON" cycle where P-MOSFET **16** ON and N-MOSFET **17** OFF.

In accordance with the present invention, regulator circuit **50** goes into sleep mode at low output current levels as follows. Hysteretic comparator **74** monitors the feedback voltage V_{FB} and goes LOW when V_{FB} exceeds a predetermined voltage value in excess of the reference voltage V_{REF}. Such a condition is indicative of the output voltage V_{OUT} exceeding a predetermined voltage value in excess of the regulated voltage V_{REG}. This over voltage condition is intentionally induced at low average output currents by providing a constant current source I_1 **72** coupled in parallel with amplifier **38**. During the over voltage condition both MOSFETS **16** and **17** are maintained OFF by way of AND gate **66** and NAND gate **68**.

Constant current source I_1 sets a minimum feedback current threshold for current comparator **39**. This sets a minimum current required in inductor L1 during each ON cycle to trip comparator **39**. In accordance with the present invention, current comparator **39** is intentionally forced to remain ON at current levels that would otherwise cause it to trip. Thus, more current is supplied to inductor L1 than is necessary to maintain the output voltage V_{OUT} at the regulated voltage V_{REG}. As a result, V_{OUT} will begin to increase beyond the regulated voltage V_{REG}, causing the feedback voltage V_{FB} to trip hysteretic comparator **74** at a predetermined voltage value in excess of V_{REF}. When comparator **74**

trips, its output goes LOW to turn both MOSFET **16** and **17** OFF to put the regulator circuit into sleep mode.

In the above-described state of operation (i.e., "sleep mode") where MOSFETs **16** and **17** are both simultaneously OFF, the output load **14** is supported substantially by output capacitor C_{OUT}. Hysteretic comparator **74** monitors the feedback voltage V_{FB} and when V_{OUT} falls such that V_{FB} has decreased by the amount of the hysteresis in comparator **74**, driver circuit **20** is taken out of sleep mode (where MOSFETS **16** and **17** are both driven OFF) so that a new ON cycle is initiated to supply current to load **14**. If the load current remains low, C_{OUT} will recharge to a voltage level in excess of V_{REG} and the feedback voltage V_{FB} will again trip comparator **74** after only a few cycles.

Thus, during light loads, control circuit **70** is adapted to turn both MOSFET **16** and MOSFET **17** OFF when they are not needed to maintain the output voltage substantially at the regulated voltage level if the output capacitor C_{OUT} is capable of doing so. When the output voltage falls below the regulated voltage level in such a mode, control circuit **70** is adapted to briefly turn switch **15** ON to recharge the output capacitor C_{OUT} back to a voltage level in excess of the regulated voltage. Therefore, V_{OUT} will oscillate between upper and lower thresholds separated by the comparator **74** hysteresis voltage multiplied by the ratio of (R_1+R_2) to R_2. The rate at which the regulator "wakes up" to recharge output capacitor C_{OUT} will automatically adapt to the load current, maintaining high efficiencies even at low output currents.

In accordance with the present invention, control circuit **70** maintains MOSFETS **16** and **17** OFF over periods of time when the output current is low enough to allow the output capacitor C_{OUT} to maintain the output voltage substantially at the regulated voltage. Typically, such periods of OFF time, wherein both MOSFETS **16** and **17** are maintained OFF even though the switching regulator is providing a regulated voltage, can extend from less than 100 microseconds to over a few seconds (respectively corresponding to a few switch cycles to over one-hundred-thousand switch cycles for a switching frequency of 100 kiloHertz). Such OFF times typically allow high efficiency to be obtained (e.g., over 90%) over an output current range in excess of 100:1. Because other components in addition the switching transistors can also be maintained OFF during such periods, even higher efficiencies can typically be obtained.

Control circuit **70** of switching regulator **50** shown in FIG. **2** is used to drive a synchronously-switched switch including MOSFETs **16** and **17**. As used herein, the term "synchronously-switched switch" refers to a switch including two switching transistors that are driven out of phase to supply current at a regulated voltage to a load. FIG. **3** shows a second embodiment of the high-efficiency control circuit of the present invention adapted to drive a switch including a switching transistor and a switching diode in a step-down configuration.

As shown in FIG. **3**, switching regulator circuit **100** includes switch **115** including P-MOSFET **116** and diode **118**. Switch **115** is driven by driver **120** including P-driver **126**. The turning-ON and turning-OFF of switch **115** is controlled by control circuit **125**. Because control circuit **125** is used to only drive one MOSFET (in contrast to control circuit **70** of FIG. **2**), it only has one output terminal **125A** (taken from the output of NAND gate **68**).

Control circuit **125** includes current comparator **39**, amplifier **38**, hysteretic comparator **74** and one-shot circuit **25**, similar to those shown in control circuit **70** of FIG. **2**. As discussed above with respect to FIG. **2**, at low average output current levels, constant current source I_1 **72** is used to intentionally overdrive the current supplied to inductor L1 so as to cause the output voltage V_{OUT} to increase beyond the regulated voltage level V_{REG} where the output can be supported substantially by output capacitor C_{OUT} for extended periods of time. During these extended time periods, P-MOSFET **116** is maintained OFF in a sleep mode so as to increase circuit efficiency.

As discussed above, control circuits **70** and **125** of FIGS. **2** and **3**, respectively, provide high-efficiency operation at low average output current levels. Such operation adapts automatically to the output current level. For example, at high output current levels during a first state of operation the switch continually alternates between an ON state and an OFF state to maintain the output voltage V_{OUT} at the regulated voltage level V_{REG}. At low output current levels during a second state of operation, where circuit efficiency would otherwise be low, the output voltage V_{OUT} is able to be maintained substantially at the regulated voltage level V_{REG} by output capacitor C_{OUT} without continuously turning the switch ON and OFF. Thus, the control circuit automatically identifies such a condition and allows the regulator circuit to go into a "sleep" mode where a minimal number of circuit components are required to be ON.

In accordance with another feature of the present invention, a regulator circuit can also incorporate a "user activated" embodiment of the control circuit of the present invention where a user input controls whether the regulator circuit is in a "sleep" mode or not. FIG. **4** is a schematic block diagram of a switching regulator circuit incorporating such a "user-activated" embodiment of the high-efficiency control circuit of the present invention for driving a switch including a pair of synchronously-switched MOSFETs in a step-down configuration.

Switching regulator circuit **150** in FIG. **4** includes push-pull switch **15**, driver **20**, output circuit **30** similar to those in circuit **50** of FIG. **2**. Control circuit **170** of regulator circuit **150** includes one-shot circuit **25**, current comparator **39** and amplifier **38** also similar to those in circuit **50** of FIG. **2**. In contrast to FIG. **2**, switch **175** (including switches **176** and **178**) is used to manually switch regulator circuit **150** into a sleep mode through user input **175A**, which may be a control signal from some other type of control circuit (not shown). Upon the closing of switch **175**, switches **176** and **178** both close.

Switch **176** is used to turn N-driver **27** OFF in sleep mode by grounding input **66A** of AND gate **66** (which normally is held HIGH by resistor **67** coupled to a positive supply). Switch **178** is used to introduce positive feedback, and therefore hysteresis, into amplifier **38** so as to allow control circuit **170** to maintain the output voltage V_{OUT} substantially at the regulated voltage level V_{REG} in sleep mode. (Resistor R_{HYS}, coupled between reference circuit **37** and the non-inverting input of transconductance amplifier **38**, is used to assist in feeding back the output of amplifier **38** into the non-inverting input of amplifier **38**.)

Switch **178** allows amplifier **38** to overdrive the supply of current to inductor L1 (through P-MOSFET **16**) so as to intentionally drive the output voltage V_{OUT} to a predetermined level in excess of the regulated voltage level V_{REG}. After being driven to such voltage level, the hysteresis in amplifier **38** maintains P-driver **26** OFF until the feedback voltage V_{FB} falls by at least the hysteresis voltage. At that point, output **39A** of current amplifier **39** goes HIGH to trigger one-shot circuit **25** so that P-MOSFET **16** is turned ON to re-charge the output capacitor C_{OUT} to the predetermined voltage level in excess of the regulated voltage level V_{REG}.

As discussed above, control circuit **170** periodically wakes up during sleep mode to turn P-MOSFET **16** ON to recharge the output capacitor C_{OUT}. It will be apparent to those of ordinary skill in art that although N-MOSFET **15** is maintained OFF during such wake-up periods, this does not have to be the case. For example, while control circuit **170** is recharging output capacitor C_{OUT}, such recharging could be accomplished by alternately turning the switching transistors OFF so as to vary the duty cycle and thereby recharge the output capacitor C_{OUT}.

Thus, regulator circuit **150** operates to increase efficiency at low current levels as in regulator circuit **50** of FIG. **2** if a user manually activates a switch. However, in contrast to regulator circuit **50** of FIG. **2**, regulator circuit **150** does not automatically adapt to the output current levels. For example, circuit **150** does not take itself out of sleep mode as the average output current increases—it relies upon user deactivation.

As discussed above, the embodiments of the control circuits of the present invention shown in FIGS. **2**–**4** include one-shot circuit **25**. In accordance with another feature of the present invention, the one-shot circuit could be replaced with other types of circuits that control the duty cycle of the power switch. For example, one-shot circuit **25** could be replaced with a pulse-width modulator circuit that provides a pulse-width modulated signal in response to a control signal. Of course, other types of circuits could be used as well.

In accordance with another feature of the present invention, one-shot circuit **25**, which provides a constant OFF-time signal, could be replaced with a one-shot circuit that provides a variable OFF-time control signal dependent upon the output voltage (V_{OUT}) and the input voltage (V_{IN}). This feature of the present invention can be used to reduce the generation and emission of audible noise from inductor L1 at low input voltages. As discussed above, such noise is associated with oscillation in the inductor current. Furthermore, this feature of the present invention can also be used to control the short circuit current if the output is short circuited.

FIG. **5** is a schematic block diagram of an exemplary switching regulator circuit incorporating the variable OFF-time control circuit of the present invention.

Switching regulator circuit **200** includes push-pull switch **15**, driver circuit **20**, current feedback circuit **210**, voltage feedback circuit **220**, feedback control circuit **230** and variable OFF-time circuit **240**. Feedback control circuit **230** monitors the output current and output voltage through inputs **232** and **234**, respectively, and provides a trigger signal at terminal **236** to initiate the OFF cycle of switch **15**. Variable OFF-time circuit **240** is used to control the OFF time as follows.

Circuit **240** includes one-shot generator **245** which is triggered by feedback control circuit **230** through terminal **236**. One-shot generator **245** includes an additional terminal **245A** coupled to control capacitor (C_{CON}) **246** whose voltage is monitored by generator **245**. In accordance with the present invention, OFF-time control circuit **250** controls the discharging of capacitor C_{CON}, and thus the capacitor voltage, so as to in turn control the OFF time of generator **245**. OFF-time control circuit **250** monitors the input and output voltages (V_{IN} and V_{OUT}) and, depending upon their values, adjusts the OFF time accordingly.

In accordance with the present invention, if the input voltage V_{IN} decreases so that the inductor L1 oscillation frequency f_{RIP} discussed above falls into an audible range, the OFF time is decreased so that f_{RIP} will accordingly increase out of an audible range. Also, if the output voltage V_{OUT} decreases due to a short circuit so that the voltage across inductor L1 is too low to allow adequate decay in inductor current during the OFF cycle, the OFF time is increased so as to avoid a current runaway condition.

In the present embodiment the discharging of control capacitor C_{CON} is regulated by controlling the magnitude of control current I_{CON}. For example, at low input voltages I_{CON} is increased by OFF-time control circuit **250** so that the voltage on control capacitor C_{CON} rapidly falls. When the control capacitor voltage falls below a predetermined value, the ON cycle of switch **15** is initiated. Additionally, at low output voltages I_{CON} is decreased by OFF-time control circuit **250** so that the voltage on control capacitor C_{CON} slowly decays to lengthen the OFF time.

Although switching regulator circuit **200** shown in FIG. **5** relies upon a particular circuit for discharging a capacitor to control the OFF time, it is apparent that other circuits for performing this same function in response to the input and output voltages can also be used. For example, if desired, an operational amplifier could be used to control the OFF-time.

Thus, a one-shot circuit has been discussed which provides a variable OFF-time control signal that adapts to the input and output voltage levels. This feature of the present invention is used to reduce the generation and emission of audible noise from the regulator circuit at low input voltage levels (i.e., reduce t_{OFF} at low input voltages) and to limit the short circuit current if the output is short circuited (i.e., increase t_{OFF} at low output voltages).

FIG. **6** is a detailed schematic diagram of an exemplary embodiment of the variable OFF-time control circuit of FIG. **5**.

OFF-time control circuit **250** accepts as inputs $V_{IN\ and}$ v_{OUT} at terminals **252** and **254**, respectively, and provides an output I_{CON} at terminal **256**. As discussed above, I_{CON} provides for the controlled discharging of a control capacitor C_{CON} coupled to terminal **256**. Control circuit **250** controls the magnitude of I_{CON}, and therefore controls the time it takes control capacitor C_{CON} to discharge. Control circuit **250** includes current source **260** (for providing current I_{CN2}), current source **270** (for providing current I_{CN1}), current compensation circuit **280** and current mirror output circuit **295**. Control circuit **250** works as follows.

Current mirror output circuit **295** is a current mirror circuit including transistor **296** and transistor **298** (having its gate **298A** connected to its drain **298B**). Circuit **295** accepts a controlled reference current I_{CREF} at input **295A** and provides a proportional output current I_{CON} related to the aspect ratios of transistor **296** and **298** (as in conventional current mirror circuits). In accordance with the present invention, I_{CREF} will be equal to either I_{CN1} or $(I_{CN1}+I_{CN2})$ depending upon voltages V_{IN} and V_{OUT} on input terminals **252** and **254**, respectively.

When $V_{IN}-V_{OUT}$ is greater than 1.5 volts, transistor **262** conducts sufficient current (from transistor **264** and current supply I_6) to hold transistor **266** OFF. With transistor **266** OFF, current I_{CN2} will be zero and current I_{CREF} will therefore be equal to current I_{CN1} provided at output terminal **270A** of current source **270**.

Current I_{CN1} is supplied by a current mirror circuit composed of transistor **272** and transistor **274** (having its gate **274A** connected to its drain **274B**). In accordance with the present invention, the reference current I_{CN1REF} flowing from transistor **274** will be equal to either I_{CN1A} or $(I_{CN1A}+I_{CN1B})$, depending upon whether transmission gate **282** is open or closed, respectively.

Transmission gate **282** is controlled by comparator **284** and will be OPEN when V_{OUT} is less than V_{TH3}. Under

OPEN conditions, I_{CN1REF} will be equal to I_{CN1A} which goes to the collector of transistor **276**. This current is derived by dividing V_{OUT} by the output divider (composed of resistors **271** and **273**) to produce voltage V_{FB1} (at the base of transistor **279**). Voltage V_{FB1} is then level shifted up by the base-emitter voltage of transistor **279** and then down by the base-emitter voltage of transistor **276** where it appears across emitter resistor **278**. The resulting transistor **276** collector current is then proportional to the output voltage V_{OUT} causing control capacitor C_{CON} to be discharged at a rate which is proportional to the discharge rate of the current in inductor L1.

Thus, when the output voltage V_{OUT} is low, such as during a fault or start-up condition, t_{OFF} will be lengthened to allow the additional time required for the current to ramp down in inductor L1.

When the output voltage V_{OUT} is greater than V_{TH3}, the output of comparator **284** closes transmission gate **282** to couple an additional compensation current I_{CN1B} to the drain of transistor **274** to provide current compensation through current compensation circuit **280**. Compensation current I^{CN1B} is equal to current I_{TRIM} minus the drain current of transistor **286**. Transistors **286** and **288** serve to mirror the collector current in transistor **290** (which is derived in a similar manner to the collector current in transistor **276** discussed above, except that voltage V_{REF} is used instead of voltage V_{FB1})

Compensation current I_{CN1B} has two purposes: 1) to serve as a trimming current to set a desired control current I_{CON} when the output voltage V_{OUT} is substantially at its regulated level, and 2) to maintain a substantially constant control current I_{CON} over a wide range of operating temperatures. During typical circuit manufacturing, variations in the resistance of resistor **278** would normally cause control current I_{CON} to be larger or smaller than desired. By trimming I_{TRIM} while in production, compensation current I_{CN1B} can be adjusted to add or subtract from the collector current (I_{CN1A}) of transistor **276** as required to provide a predetermined control current I_{CON}. Additionally, if resistors **278** and **292** are matched (i.e., designed and fabricated similarly), then control current I_{CON} variations due to the temperature variation of the resistance of resistor **278** will be substantially cancelled by a corresponding change in the resistance of resistor **292**.

If the output voltage V_{OUT} is less than voltage V_{TH3}, the output of comparator **284** opens transmission gate **282** and thus inhibits current compensation. This ensures that control current I_{CON} will approach zero as the output voltage V_{OUT} approaches zero, thus guaranteeing control of the inductor current I_L during an output short circuit.

When V_{IN} falls to the point that V_{IN}-V_{OUT} is less than 1.5 volts, the current in transistor **262** no longer holds transistor **266** OFF. As V_{IN} decreases further, transistor **266** adds additional current (I_{CN2}) into current mirror output circuit **295**, thereby increasing control current I_{CON} and, thus, reducing t_{OFF}. This in turn stabilizes the operating frequency as V_{IN} decreases, reducing potential audibility problems. Current source I_7 determines the maximum current that transistor **266** adds to control current I_{CON}.

Thus, when V_{IN} falls so that V_{IN}-V_{OUT} is less than 1.5 volts (e.g., when a battery is nearly discharged), t_{OFF} will be reduced to increase the oscillation frequency of the regulator circuit so that the generation and emission of audible noise is reduced.

Although variable OFF-time control circuit **250** was discussed above with respect to a regulator circuit which includes push-pull switch **15** and driver **20**, it will be apparent that the variable OFF-time feature of the present invention could be used in other regulators as well. For example, this feature could also be used in the regulator circuits of FIGS. **3** and **4** and other circuits that employ one-shot generators to provide a regulated voltage.

FIG. **7** is a detailed schematic block diagram of an exemplary switching regulator circuit incorporating both the variable OFF-time feature and the high-efficiency control circuit of the present invention to drive a switch including a pair of synchronously-switched MOSFETs in a step-down configuration.

Switching regulator **300** includes push-pull switch **15**, driver **20**, output circuit **30** and control circuit **350**. Control circuit **350** includes one-shot generator **245**, variable OFF-time control circuit **250** for controlling the OFF cycle time and comparator **74** for providing high-efficiency operation at low average output current levels. Switching regulator **300** works as follows.

When the load current exceeds, for example, approximately 20 percent of the maximum output current, the loop operates in a continuous mode wherein comparator **74** does not override output **245A** of one-shot generator **245**. With V_{IN}-V_{OUT} greater than 1.5V, operation is substantially similar to that described for FIG. **1**. The inductor current is sensed by means of the voltage drop across resistor R_{SENSE}, and the threshold for the current comparator **39** is set by the voltage drop across resistor R_3. Built-in offset V_{OS} (e.g., about 10 mv) levelshifts feedback voltage V_{FB} slightly below reference voltage V_{REF}, thus keeping the output of comparator **74** HIGH in this mode. When the voltage across resistor R_{SENSE} exceeds the threshold across resistor R_3, the output of comparator **39** goes HIGH and the RBAR input of RS flip-flop **310** goes LOW, resetting RS flip-flop **310**, and thus, initiating the switch OFF cycle.

During the OFF cycle, switch signal V_{SWB} is HIGH, which turns P-MOSFET **16** OFF, N-MOSFET **17** ON and allows I_{CON} to discharge control capacitor C_{CON}. The OFF time, t_{OFF}, is in turn determined by the time it takes control capacitor C_{CON} to discharge from its initial voltage to V_{TH1}, coupled to the non-inverting input of comparator **312**. When control capacitor C_{CON} discharges to voltage V_{TH1}, the output of comparator **312** goes LOW, thus setting RS flip-flop **310** and initiating the next ON cycle. Voltage V_{TH1} is higher than voltage V_{TH2}, thus causing the output of comparator **315** to remain LOW in the continuous mode.

In accordance with present embodiment, the OFF time is controlled by variable OFF-time control circuit **250** described above with respect to FIGS. **5** and **6**. Accordingly, circuit **250** includes inputs **252** and **254** coupled to V_{IN} and V_{OUT}, respectively, to monitor those voltages.

Current source I_1 sets a minimum voltage threshold across resistor R_3 for current comparator **39**. This sets a minimum current required in inductor L1 during each ON cycle to trip comparator **39**. If the resulting average inductor current flowing to the output is greater than the load current, then output voltage V_{OUT} will begin to increase, causing feedback voltage V_{FB} to trip the hysteretic comparator **74**. Of course, the inductance of inductor L1 and OFF time t_{OFF} are preferably chosen so that the inductor ripple current is not below zero when such tripping occurs. When comparator **74** trips, its output goes LOW and overrides the Q output of RS flip-flop **310**, immediately switching switch signal V_{SWB} high. As discussed above, this automatically initiates the beginning of the "sleep" mode of operation.

In sleep mode, capacitor C_{CON} discharges as before, but does not initiate a new switch ON cycle when comparator **312** trips. As discussed above, this is because until feedback

voltage V_{FB} has fallen by the amount of hysteresis in comparator **74**, the LOW at output **74A** forces switch signal V_{SWB} to remain HIGH through NAND gate **316**. Accordingly, control capacitor C_{CON} continues to discharge below voltage V_{TH2}, causing output **315A** of comparator **315** to go HIGH. This in turn causes the N-MOSFET **17** as well as the P-MOSFET **16** to be turned OFF. In addition, unused circuit components such as amplifier **38** and comparators **39** and **312** are also turned OFF when the regulator circuit is in sleep mode. As discussed above, this decreases bias currents substantially during sleep mode, further increasing efficiency at low output current levels.

During the extended off times in sleep mode, much of the regulator and both MOSFETS **16** and **17** are turned off, and the output load is supported substantially by output capacitor C_{OUT}. However, when the output voltage V_{OUT} falls such that the feedback voltage V_{FB} has decreased by the amount of hysteresis in comparator **74**, all circuit components are again turned on and a new ON cycle is initiated to supply current to the output. If the load current remains low, output capacitor C_{OUT} will recharge, and the feedback voltage V_{FB} will again trip comparator **74** after only a few switch cycles. Thus, during light load conditions, the output voltage V_{OUT} will oscillate between upper and lower thresholds values, as discussed above.

Whenever P-MOSFET **16** is ON, its gate-to-source voltage also appears across MOSFET **334**, turning MOSFET **334** ON. This pulls the drain of MOSFET **334** HIGH, and inhibits N-drive **27**. Following a LOW-to-HIGH V_{SWB} transition, the voltage on the gate of P-MOSFET **16** must rise to a level where MOSFET **334** is conducting less than current source **335** before the drain voltage of MOSFET **334** falls and allows the N-MOSFET **17** to be turned ON. Current I^{M1} is purposely made small so that the gate of MOSFET **334** must rise to within 2 volts of the input voltage V_{IN} before the drive is enabled, ensuring that the P-MOSFET is completely OFF when N-MOSFET **17** turns ON. In a similar manner, MOSFET **332** and current source I_{M2} **333** ensure that the N-MOSFET **17** is completely OFF when the P-MOSFET **16** turns ON. This prevents simultaneous conduction regardless of the driver speeds or MOSFET sizes, ensuring maximum possible efficiency. This feature of the present embodiment is discussed in more detail in copending commonly-assigned U.S. patent application (LT-20) Ser. No. 07/893,523, filed Jun. 4, 1992, which is hereby incorporated by reference in its entirety. If desired, the control circuit of the present invention can also include circuitry for accommodating transient switch signals as described in copending commonly-assigned U.S. patent application (LT-20CIP) Ser. No. 08/035,423, filed concurrently herewith, which is also hereby incorporated by reference in its entirety.

Schottky diode D2 coupled across N-MOSFET 17 shown in FIG. 7 only conducts during the deadtime between the conduction of MOSFETS 16 and 17. Diode D2's purpose is to prevent the body diode of N-MOSFET 17 from turning on and storing charge during the deadtime, which could reduce efficiency (e.g., by approximately 1 percent) in some cases. Diode D2 preferably is selected with a forward voltage of less than about 0.5 volts when conducting the maximum output current.

In accordance with the present invention, the control circuit shown in FIG.7, when incorporated into a 5-volt synchronous step-down switching regulator, is capable of achieving over 90 percent efficiency (for an input voltage of approximately 10 volts) while the output current varies over two orders of magnitude (e.g., 20 mA to 2 A). Under some operating conditions (e.g., for an input voltage of 6 volts) efficiencies of over 95 percent can be maintained over such current levels. Such a control circuit is particularly useful in notebook and palm-top computers, portable instruments, battery-operated digital devices, cellular telephones, DC power distributions systems and GPS systems.

As discussed above with respect to FIG. **1**, a disadvantage of prior art control circuit **10** is that at low output currents the current in inductor L1 may reverse polarity if during t_{OFF} the current ramps down too much. This may result in power being pulled from the load to ground, through N-MOSFET **17**, with an associated reduction in circuit efficiency. In accordance with a still further feature of the present invention, the control circuit can include a circuit for turning OFF the N-MOSFET to prevent such power from being pulled from the load if the inductor current reverses polarity.

FIG. **8** is a schematic block diagram of an exemplary switching regulator circuit incorporating a circuit of the present invention for preventing reversals in the polarity of the current in the output inductor of the regulator from drawing power from the load.

Switching regulator **400** includes push-pull switch **15**, driver circuit **20** and output circuit **30** similar to those of FIG. **1**. Circuit **400** also includes an embodiment **470** of the high-efficiency control circuit of the present invention for preventing reversals in the polarity of output inductor L1 current from drawing power from the load.

Control circuit **470** includes one-shot circuit **25**, current comparator **39** and transconductance amplifier **38** similar to those of FIG. **1**. In addition to those components, control circuit **470** also includes comparator **471** and gate **472** for preventing reversals in inductor current polarity from drawing power from the load at low average current levels. Control circuit **470** works as follows.

When output **25***a* of one-shot circuit goes HIGH to turn P-MOSFET **16** OFF and N-MOSFET **17** ON, the inductor current I_L begins to ramp down. During low average output currents, this current may ramp down towards zero and, eventually, may go negative. Control circuit **470** works by monitoring the inductor current I_L, through current feedback signal I_{FB2}, and turns N-MOSPET **17** OFF before such current reversals can occur. This prevents N-MOSFET **17** from drawing power from the load to ground.

Comparator **471** includes an input **471***a* adapted to monitor inductor current I_L by way of current feedback signal I_{FB2}. When current feedback signal I_{FB2} falls below current I_4 applied to input **471***b* of comparator **471**, comparator output **471***c* goes LOW and, therefore, turns N-MOSFET **17** OFF by way of NAND gate **472**. The turning OFF of N-MOSFET **17** prevents current reversals in inductor current I_L from drawing power from load **14** to ground through N-MOSFET **17**.

After N-MOSFET **17** is turned OFF, it will again be allowed to turn ON as soon as feedback current I_{FB2} exceeds current I_4 to cause comparator output **471***c* to go HIGH. Generally, comparator output **471***c* will again go HIGH after one-shot circuit **25** turns P-MOSFET **16** ON, which, in turn, causes-the inductor current I_L to again ramp up. Such ramping up will allow current feedback signal I_{FB2} to exceed I_4 and, therefore, cause comparator output **471***c* to go HIGH. While comparator **471***c* is HIGH, one-shot circuit **25** solely controls the turning ON of N-MOSFET **17**.

Thus, control circuit **470** includes circuitry for intentionally holding N-MOSFET **17** OFF during periods when current reversals would otherwise allow power to be drawn from the load. This feature of the present invention can increase circuit efficiency at low average output current levels when current reversals are most like to occur.

It will be apparent to those of ordinary skill in the art that although comparator **471** monitors the inductor current I_L through feedback current I_{FB2}, other means of detecting current reversals in the inductor current I_L could be used as well. For example, comparator **471** could monitor current feedback signal I_{FB1} just as well so that only one type of current feedback signal is employed in control circuit **470**. Additionally, many others means of generating a feedback signal indicative of current reversal in inductor current I_L could be used as well (see, e.g., resistor R_{SENSE} in FIG. **7**).

The high-efficiency control circuit of the present invention was discussed above with respect to FIGS. **1–8** wherein the switching regulator was configured in a voltage step-down configuration. It will be apparent that the control circuit of the present invention could be used in other configurations as well. For example, FIG. **9** shows a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a voltage step-up configuration.

Switching regulator-**500** includes synchronously-switched switch **15'** wherein the drains of P-channel MOSFET **16** and N-channel MOSFET **17** are coupled together and to one side of inductor L1. The other side of inductor L1 is coupled to input V_{IN}. Control circuit **70** drives driver circuit **20'** including inverting P-driver **26'** and inverting N-driver **27'**, which in turn drive P-channel MOSFET **16** and N-channel MOSFET **17**, respectively.

Thus, as shown in FIG. **9**, the control circuit of the present invention can be used in switching configurations wherein an input voltage V_{IN} is stepped up to a regulated output voltage V_{OUT}. As is the case with the step-down configurations shown in FIGS. **2–8**, the control circuit of FIG. **9** can be used in other types of step-up configurations as well. For example, one-shot circuit **25** shown in FIG. **9** can include an additional input for monitoring the input voltage V_{IN} to reduce the generation and emission of audible noise from inductor L1 at low input voltages as discussed above with respect to FIGS. **5** and **6**. Also, switching regulator **500** can include circuitry to hold P-MOSFET **16** OFF during periods when the polarity of inductor current I_L would otherwise reverse, as discussed above with respect to FIG. **8**.

FIG. **10** shows a schematic block diagram of a switching regulator circuit incorporating the high-efficiency control circuit of the present invention in a voltage polarity-inversing configuration.

Switching regulator **600** includes switch **15"** wherein the drain of P-channel MOSFET **16** is coupled to one side of inductor L1 and to VA through diode **D601**. The other side of inductor L1 is coupled to ground. The source of P-channel MOSFET **16** is coupled to the positive input voltage V_{IN}. Control circuit **70'** drives driver circuit **20"** including P-driver **26** which, in turn, drives P-channel MOSFET **16**.

Control circuit **70'** operates substantially similar to control circuit **70** discussed above except for the following. Voltage feedback to control circuit **70'** is provided by resistors **R1** and R2 and amplifier **602**. Amplifier **602** inverts the negative polarity voltage at V_{OUT} to provide a positive polarity feedback voltage to control circuit **70'**.

Thus, as shown in FIG. **10**, the control circuit of the present invention can be used in switching configurations wherein an input voltage V_{IN} is inverted to a regulated output voltage of opposite polarity V_{OUT}. As is the case with the step-down configurations shown in FIGS. **2–8**, the control circuit of FIG. **10** can be used in other types of polarity-inversing configurations as well. For example, one-shot circuit **25** shown in FIG. **10** can include an additional input for monitoring the input voltage V_{IN} to reduce the generation and emission of audible noise from inductor L1 at low input voltages. Furthermore, one-shot circuit **25** can include an input for monitoring the output voltage V_{OUT} to control the short circuit current if the output is short circuited as discussed above with respect to FIG. **5** and **6**. Also, if regulator **600** was synchronously switched and included an N-MOSFET instead of **D601**, the regulator could include circuitry to hold such an N-MOSFET OFF during periods when the polarity of inductor current I_L would otherwise reverse, as discussed above with respect to FIG. **8**.

It will be apparent to those of ordinary skill in the art that although the present invention has been discussed above with reference to a hysteretic voltage comparator for generating the sleep mode control signal to cause the switching regulator to go into and awake from the sleep-mode, other means for performing the same function are also possible. For example, if desired, the sleep mode control signal could be generated in response to a monitored output current. Furthermore, the switching regulator could be taken out of the sleep mode a predetermined time period after going into such a mode, instead after the output voltage falls below a predetermined threshold voltage, as illustrated above.

It will also be apparent that although the present invention has been discussed above with reference to FIGS. **1–10**, wherein the power switches were either a pair of complementary MOSFETS (i.e., one p-channel and one n-channel) or a single p-channel MOSFET (FIG. **3**), the present invention is applicable to other types of switches as well. For example, the power switch could include a pair of N-channel MOSFETS, a pair of P-channel MOSFETS, or bipolar junction transistors.

Thus, a control circuit and method for maintaining high efficiency over broad current ranges in a switching regulator circuit has been provided.

One skilled in the art will thus appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.

What is claimed is:

1. A circuit for controlling a switching voltage regulator, the regulator having (1) a switch coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output for supplying current at a regulated voltage to a load which includes an output capacitor, the circuit comprising:

a first circuit for monitoring the output to generate a first feedback signal;

a second circuit for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the first feedback signal to vary the duty cycle of the switching transistors to maintain the output at the regulated voltage; and

a third circuit for generating a second control signal during a second state of circuit operation to cause both switchin transistors to be OFF for a first period of time during which the output capacitor maintains the output substantially at the regulated voltage.

2. The circuit of claim **1** wherein the second control signal is generated in response to the first feedback signal.

3. The circuit of claim **2** wherein the circuit changes from the second to the first state of operation in response to the magnitude of the first feedback signal falling below a first threshold level.

4. The circuit of claim **3**, wherein the circuit changes from the first to the second state of operation in response to the magnitude of the first feedback signal exceeding a second threshold level greater than the first threshold level.

5. The circuit of claim 4, wherein the first feedback signal is a voltage feedback signal and the third circuit includes a voltage comparator having hysteresis.

6. The circuit of claim 5, wherein the current consumed by the switching voltage regulator is reduced during the second state of operation.

7. The circuit of claim 2, wherein the second circuit includes:

a one-shot circuit for generating the first control signal, the first control signal being generated over a second period of time during a switch cycle.

8. The circuit of claim 7, wherein the second period of time is a predetermined time period.

9. The circuit of claim 8, wherein the second circuit includes a fourth circuit for monitoring the current supplied to the load to generate a current feedback signal.

10. The circuit of claim 9, wherein the switch is adapted to be coupled to an inductor and the fourth circuit monitors the inductor current to generate the current feedback signal.

11. The circuit of claim 10, wherein the fourth circuit compares the current feedback signal to a reference current value and triggers the one-shot circuit when the current feedback signal exceeds the reference current value.

12. The circuit of claim 11, wherein the fourth circuit includes a current comparator for triggering the one-shot circuit, the current comparator having a first input coupled to receive the current feedback signal and a second input coupled to a current source for providing the reference current value.

13. The circuit of claim 12, wherein the current source includes:

a transconductance amplifier supplying a current substantially proportional to the difference in voltage between the first feedback signal and a constant voltage; and

a constant current source coupled in parallel with the transconductance amplifier.

14. The circuit of claim 7, wherein the second period of time is dependent upon the input voltage.

15. The circuit of claim 14, wherein the switch is coupled to an inductor, and wherein the second period of time is decreased in response to a decrease in the input voltage, whereby the oscillation frequency of the ripple current through said inductor is increased from an audible frequency to one that does not generate substantial user noise.

16. The circuit of claim 7, wherein the second period of time is dependent upon the voltage at the load.

17. The circuit of claim 16, wherein the switch is coupled to an inductor, and wherein the second period of time is increased in response to a decrease in the voltage at the load, whereby the total decrease in current through said inductor is increased while the first control signal is generated.

18. The circuit of claim 7, wherein the one-shot circuit is maintained substantially OFF during the second state of operation, whereby the efficiency of the switching regulator circuit is increased as the circuit changes from the first to the second state of operation.

19. The circuit of claim 12, wherein the current comparator is maintained substantially OFF during the second state of operation, whereby the efficiency of the switching regulator circuit is increased as the circuit changes from the first to the second state of operation.

20. The circuit of claim 1, wherein the third circuit includes a user-activated switch and wherein the second control signal is generated in response to activation of the user switch.

21. The circuit of claim 20 wherein:

the second circuit includes a transconductance amplifier supplying a current substantially proportional to the difference in voltage between the feedback signal and a constant voltage during the first state of operation; and

wherein activation of the user switch introduces hysteresis into the transconductance amplifier.

22. The circuit of claim 20, wherein the second circuit includes:

a one-shot circuit for generating the first control signal, the first control signal being generated over a second period of time during a switch cycle.

23. The circuit of claim 22, wherein the second period of time is a predetermined time period.

24. The circuit of claim 23, wherein the second circuit includes a fourth circuit for monitoring the current supplied to the load to generate a current feedback signal.

25. The circuit of claim 24, wherein the fourth circuit compares the current feedback signal to a reference current value and triggers the one-shot circuit when the current feedback signal exceeds the reference current value.

26. The circuit of claim 22, wherein the second period of time is dependent upon the input voltage.

27. The circuit of claim 26, wherein the switch is coupled to an inductor, and wherein the second period of time is decreased in response to a decrease in the input voltage, whereby the oscillation frequency of the ripple current through said inductor is increased from an audible frequency to one that does not generate substantially user noise.

28. The circuit of claim 22, wherein the second period of time is dependent upon the voltage at the load.

29. The circuit of claim 28, wherein the switch is coupled to am inductor, and wherein the second period of time is increased in response to a decrease in the voltage at the load, whereby the total decrease in current through said inductor is increased while the first control signal is generated.

30. The circuit of claim 22, wherein the one-shot circuit is maintained substantially OFF during the second state of operation, whereby the efficiency of the switching regulator circuit is increased as the circuit changes from the first to the second state of operation.

31. The circuit of claim 1, wherein the circuit is adapted for controlling a switching voltage regulator circuit having first and second switching transistors coupled in series between an input voltage and ground, wherein the first and second switching transistors are commonly coupled at the output terminal, and wherein the input voltage is higher than the voltage at the load, whereby the switching voltage regulator is a step-down voltage regulator.

32. The circuit of claim 1, wherein the circuit is adapted for controlling a switching voltage regulator circuit wherein the input voltage is lower than the voltage at the load, whereby the switching voltage regulator is a step-up voltage regulator.

33. The circuit of claim 1, wherein the circuit is adapted for controlling a switching voltage regulator circuit wherein the input voltage has an opposite polarity than the voltage at the load, whereby the switching voltage regulator is a polarity-inversing voltage regulator.

34. A method for controlling a switching voltage regulator, the regulator having (1) a switch coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output for supplying current at a regulated voltage to a load which includes an output capacitor, the method comprising the steps of:

(a) monitoring the output to generate a first feedback signal;

(b) varying the duty cycle of the switching transistors in response to the first feedback signal to maintain the

output at the regulated voltage during a first state of circuit operations;

(c) turning both switching transistors OFF for a first period of time following the first state of circuit operation so as to allow the output capacitor to maintain the output substantially at the regulated voltage by discharging during a second state of circuit operation; and

(d) turning at least one of said switching transistors ON to recharge the output capacitor following the second state of circuit operation.

35. A circuit for controlling a switching voltage regulator, the regulator having (1) a switch coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output for supplying current at a regulated voltage to a load which includes an output inductor, the circuit comprising:

a first circuit for monitoring the output to generate a first feedback signal;

a second circuit for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the first feedback signal to vary the duty cycle of the switching transistors to maintain the output at the regulated voltage; and

a third circuit for monitoring the current to the load to generate a second control signal during a second state of circuit operation to cause one of said switching transistors to be maintained OFF when the magnitude of the monitored current falls below a current threshold.

* * * * *

EXHIBIT C

FILED UNDER SEAL